NorthStar Computers Inc.
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North Star
16K Ram Board

RAM-16-DOC
Revision 2

North Star

16K RAM Board

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INTRODUCTION

The North Star 16K byte RAM board (RAM-16-A) is compatible with S-100 computers. The board will operate at full speed with both 8080 and Z80 microcomputers, even with 4 MHz operation. The industry standard 16-pin 4027 RAM chip (200 nanoseconds access) is used. A parity option is available for use with the RAM-16-A. The RAM-16-A may be addressed to any 16K region beginning at any 8K boundary. The RAM-16-A has a bank switching feature which allows more than 64K bytes of RAM to be used in the computer, and also facilitates special software applications such as time-sharing.

If you have purchased the RAM-16-A as a kit, then first skim the entire manual. Be sure to carefully read the Assembly Information section before beginning assembly. If you have purchased the RAM-16-A in assembled form, you may skip the Assembly section. Regardless of whether you purchased the RAM-16-A as a kit or assembled, be sure to read the Configuration section which discusses how to configure the RAM-16-A for each individual application.

CAUTIONS

1. Correct this document from the errata sheets, if any, before doing anything else.

2. Assembly of this product from a kit is a complex, demanding project. It should not be attempted without previous kit building experience.

3. Do NOT insert or remove any boards from the computer when the power is on. Note that power is not completely off until the capacitors have discharged, several seconds after turning off the computer power switch.

4. Do NOT insert or remove IC's from any board while the power is turned on.

5. Be sure that all IC's are inserted in their correct positions and with correct orientation before turning on the power. Be sure that all IC pins are correctly inserted in the socket and are not bent under the IC and are not outside the socket.

6. Carefully observe the prescribed rules for handling the MOS type integrated cirucits. The handling procedures are described in the Assembly Information section of this manual.

LIMITED WARRANTY

North Star Computers, Inc. warrants the electrical and mechanical parts and workmanship of this product to be free of defects for a period of 90 days from date of purchase. If such defects occur, North Star Computers, Inc. will repair the defect at no cost to the purchaser. This warranty does not extend to defects resulting from improper use or assembly by purchaser, nor does it cover transportation to the factory. Also, the warranty is invalid if all instructions included in the accompanying documentation are not carefully followed. Should a unit returned for warranty repair be deemed by North Star Computers, Inc. to be defective due to purchaser's action, then a repair charge not to exceed $30 without purchaser's consent will be assessed. ANY UNIT OR PART RETURNED FOR WARRANTY REPAIR MUST BE ACCOMPANIED BY A COPY OF THE ORIGINAL SALES RECEIPT. This limited warranty is made in lieu of all other warranties, expressed or implied, and is limited to the repair or replacement of the product. No warranty, expressed or implied, is extended concerning the completeness, correctness, or suitability of the North Star equipment for any particular application. There are no warranties which extend beyond those expressly stated herein.

OUT OF WARRANTY REPAIR

If your unit is out of warranty and you are unsuccessful at diagnosing or repairing the problem, out-of-warranty service may be arranged with a local dealer or other experienced local computer technician. Alternatively, any North Star products may be shipped PREPAID to the North Star address with a clear written description of the problem. Include as many details as possible about the problem and about your system configuration. Your unit will be returned, C.O.D., within 30 days after receipt by North Star. Out-of-warranty repair service is billed at the rate of $25.00 per hour. If you wish to place an upper limit on the amount of time spent on your unit, mention this in the written description.

RAM-16-A PARTS LIST

1	RAM-16-A Manual
1	RAM-16-A printed circuit board, 5" x 10"
2	20-pin IC sockets
39	16-pin IC sockets
21	14-pin IC sockets
1	14-pin DIP header
1	8-position DIP switch
1	delay line, DDU-4-7781 or STTLDM-400
1	+5 volt regulator, 7805 or 340T-5
1	+12 volt regulator, 7812 or 340T-12
1	-5 volt regulator, 79L05
1	heat sink, 6106B-14
1	heat sink, 6107B-14
2	6-32x3/8" machine screws
2	#6 lock washers
2	6-32 nuts

Integrated Circuits

2	74LS00	1	74LS373
1	74LS02	1	74LS393 (or 74393)
1	74LS08	1	7402
1	74LS13	1	74S00
2	74LS14	2	74S10
1	74LS30	1	74S30
1	74LS74	1	74S74
1	74LS75	1	74S113
1	74LS123 (or 74123)	1	74S138
2	74LS132	1	74S175
1	74LS241	32	4027-3 (MOS)
3	74LS352		

Resistors

8	2.2K ohm	1/4W	red-red-red
1	220 ohm	1/4W	red-red-brown
3	330 ohm	1/4W	orange-orange-brown
1	470 ohm	1/4W	yellow-violet-brown
1	10K ohm	1/4W	brown-black-orange
1	18K ohm	1/4W	brown-gray-orange
8	22 ohm	1/4W	red-red-black
1	4.7K ohm resistor network, 10-pin		

Capacitors

2	.0047uF	dipped mylar
1	33pF	dipped mica (may be marked "330J03")
3	47pF	ceramic disc
1	100pF	dipped mica
5	6.8uF	dipped tantalum
2	2.2uF	dipped tantalum
60	.047uF	ceramic disc

PARITY OPTION PARTS LIST

1	74LS109 IC
2	74LS280 IC
1	75452 IC (8-pin)
4	4027-3 IC (MOS)
5	16-pin IC sockets
2	14-pin IC sockets
1	8-pin IC socket
1	220 ohm 1/4W resistor (red-red-brown)
1	LED

ASSEMBLY INFORMATION

Read completely through each section before beginning the first instruction step of that section. Perform all operations in the sequence indicated. Read each step entirely, including any notes that accompany the step, before beginning to follow the step.

WORK AREA AND TOOLS

Start with a clean, well-lit and well-ventilated area to work. The area should be large enough to accommodate the kit, tools, parts and assembly instructions. Suggested tools are: screwdrivers, needle-nose pliers, diagonal cutters, soldering iron, solder, and masking tape. A number of tests will require using a VOM (ohmmeter-voltmeter), or VTVM. Also highly desirable, but not necessary, are an IC inserter, a screw-holding screwdriver, an oscilloscope or logic probe, and an extender card. [Note that if you do not have an oscilloscope or logic probe, waveforms can be detected by one of the procedures described in Appendix 1.]

SOLDERING TIPS

For best results use a 15 to 25 watt soldering iron or an iron with a temperature controlled tip (approximately 700 degrees). The tip should be no wider than the solder pads on the printed circuit board. Use only a fine gauge rosin core solder (60/40 or 63/37). Do NOT use acid core solder as this can severely damage a printed circuit board. When soldering, keep the soldering iron tip on the pad just long enough for the solder to completely flow. If the solder does not draw up the wire then more solder is required. Do not use so much solder that it overflows the pad. If a solidified joint is not shiny, it may be a cold solder joint and should be remelted. The soldering iron tip should be cleaned frequently by wiping on a damp sponge

When you have completed assembly of a board, inspect it for unintended solder connections or "bridges", as well as unsoldered leads. After soldering, it is recommended that the rosin flux be removed from the board using flux remover, FREON or paint-thinner type solvent. This will make looking for soldering problems easier and give the board a clean, professional appearance

IC SOCKET INSTALLATION

Integrated circuit (IC) sockets can be installed by first inserting them into the printed circuit board, then placing another flat board over the IC sockets and finally turning over this sandwich. Be sure that each IC socket is inserted into the proper location and is oriented such that pin 1 of the socket corresponds to the pin 1 indication on the PC board layout legend. (Refer to figure 1A to identify pin 1 on an IC socket.) To solder IC sockets, first solder just two opposite corner pins

for all sockets being installed. Then remelt the corner connections while applying pressure down on the board. This will remove any gaps that may be present between the IC sockets and the PC board. Finally, solder the remaining pins of the IC sockets.

DIP HEADER SOLDERING

When making jumper connections on a DIP header, solder resistor or capacitor lead snippings between the leads to be connected. When more than two pins are to be connected together, bend a single wire so that it routes to each pin, and solder each pin once. Insert the header in an IC socket on a PC board to hold it during soldering. Overheating the pins with the soldering iron will melt the plastic of the header. If there are multiple jumpers on a header, make sure that no unintended connections are made by carefully routing the jumpers, or by insulating each jumper with some wire insulation.

RESISTOR AND CAPACITOR INSTALLATION

To install resistors or capacitors, first make right angle bends in the leads to fit the PC board hole spacing. (Some capacitor leads are already appropriately spaced and do not need bending.) Then insert the leads as far as possible through the correct holes in the PC board and spread the leads slightly on the solder side of the board to keep the part in place. After a group of resistors or capacitors has been inserted, then solder the leads on the solder side of the board and snip off the excess leads as close to the board as possible. Use caution to avoid eye injury from flying bits of wire. Save the lead clippings for later use in making jumper connections.

PRINTED CIRCUIT BOARD LAYOUT

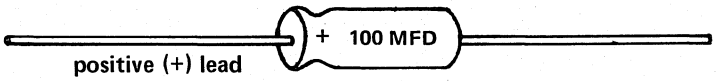
The white component layout legend is printed on the component side of a printed circuit (PC) board. All components are inserted from this side (component side) and soldered on the other side (solder side). Locations on the PC board are identified by two-character codes as marked on the board: a digit followed by a letter indicating the horizontal and vertical coordinates of the location. Note that in North Star kits, IC's can be found on styrene pads in positions corresponding to their intended locations on the PC board.

Pin numbering conventions for the S-100 edge pins are as follows: When viewing the component side of the board (with the pin edge facing down), pins 1,2, ... 50 range from left to right. When viewing the solder side of the board, pins 100, 99, ..., 51 range from left to right.

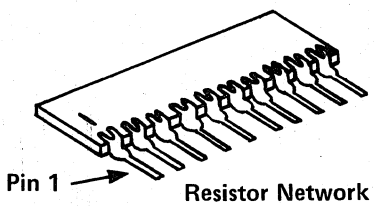
MOS INTEGRATED CIRCUIT HANDLING

Some North Star PC boards use some MOS-type IC´s. These parts are identified as such in the instructions. MOS devices can be damaged by static electricity discharge, so special handling is necessary to protect them. Handle MOS devices as little as possible and avoid touching the pins. Place the conductive foam or tube which contains the MOS device onto the PC board before removing the device from the foam or tube. Also, be sure both hands are touching the foam or tube when the device is removed from the foam or tube.

Once an MOS device has been installed in a PC board, handle the board as little as possible. Of course, never insert or remove any IC while power is applied to the board, and never remove or insert a PC board while power is applied to the motherboard.

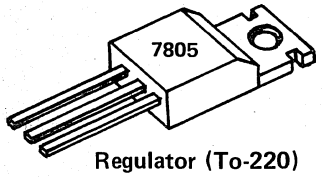


Axial Lead
Electrolytic Capacitor

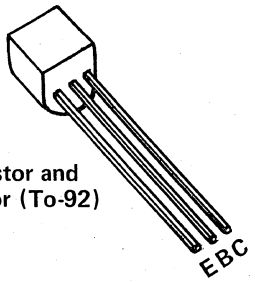


Resistor Network

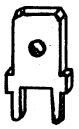
Resistor



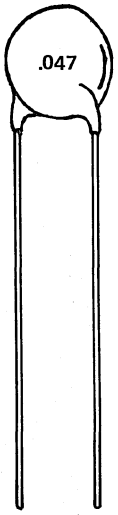
Regulator (To-220)



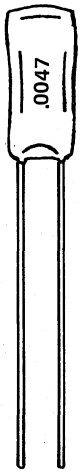
Transistor and
Regulator (To-92)



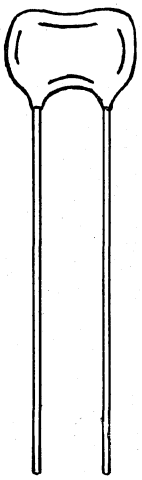
Quick-Connect
Lug



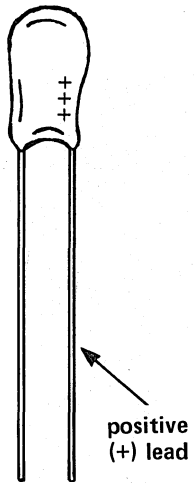
Ceramic
Disc
Capacitor



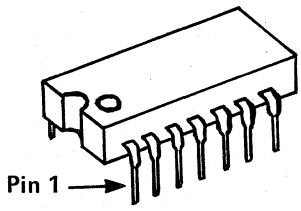
Dipped
Mylar
Capacitor



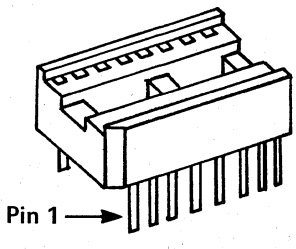
Dipped
Mica
Capacitor



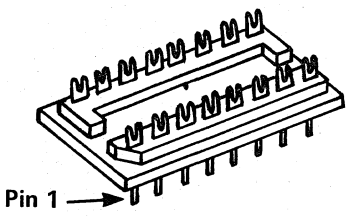
Dipped
Tantalum
Capacitor



Integrated Circuit (IC)



IC Socket



DIP Header

Figure 1A. Identification and orientation of components.

RAM BOARD ASSEMBLY

Before beginning assembly of the RAM board, first check that you have all the parts listed in the parts list. This manual applies to the RAM-16-A3 board revision - check the PC board marking to be sure you do not have a RAM-16-A2 board. Note that in the following instructions, "left" and "right" refer to those directions when viewing the component side of the PC board with the 100-pin connector facing down.

R1. Using an ohmmeter, check for open circuits between the pair of solder pads for each of the following six capacitor locations: C1, C2, C3, C4, C5, and C6. If any shorts are found, locate and correct the problem or return the PC board for replacement.

R2. Insert and solder the two 20-pin IC sockets at locations 8D and 17E on the PC board. Follow the procedure described in the Assembly Information section. Be sure the sockets are installed with the correct orientation (all the IC's have pin 1 toward the top of the board.

R3. Insert and solder the thirty-nine 16-pin sockets with correct orientation. Do not install a socket at the switch position (7A). Do not install any sockets in the positions reserved for the parity option unless you will be assembling the parity option at this time. The parity option sockets are located at positions 3A, 9A, 9B, 9C, and 9D.

R4. Insert and solder the twenty-one 14-pin sockets with correct orientation. Do not install sockets at locations 10E or 15E, unless you are assembling the parity option at this time.

R5. Now check all the solder joints for possible solder bridges between adjacent solder pads, unsoldered connections, or cold solder joints.

R6. Insert and solder the following resistors:

Resistor	Value	Size	Location	Color-code
R1	2.2K	1/4W	0A	red-red-red
R3	330	1/4W	2D	org-org-brn
R4	2.2K	1/4W	7A	red-red-red
R5	18K	1/4W	1A	brn-gry-org
R6	470	1/4W	1B	yel-vio-brn
R7	10K	1/4W	2A	brn-blk-org
R8	2.2K	1/4W	7A	red-red-red
R9	2.2K	1/4W	3D	red-red-red
R10	330	1/4W	10E	org-org-brn
R11	2.2K	1/4W	6A	red-red-red
R13	2.2K	1/4W	5C	red-red-red

( )	R14	2.2K	1/4W	6C	red-red-red
( )	R15	2.2K	1/4W	1B	red-red-red
( )	R16	22	1/4W	8B	red-red-blk
( )	R17	22	1/4W	8B	red-red-blk
( )	R18	22	1/4W	8B	red-red-blk
( )	R19	22	1/4W	8B	red-red-blk
( )	R20	22	1/4W	8B	red-red-blk
( )	R21	22	1/4W	8B	red-red-blk
( )	R22	22	1/4W	8B	red-red-blk
( )	R23	22	1/4W	8B	red-red-blk
( )	R24	330	1/4W	12E	org-org-brn

R7. Insert and solder the single-in-line (SIP) resistor network labeled RN1 on the layout legend at location 16E. Orient the SIP so the end marked with a "1" (sometimes this end has a beveled corner) corresponds to the end marked with a dot on the layout legend.

Save the resistor R12 (220 ohm, red-red-brn) for future special DMA applications. See the Special DMA Applications section for details. Note that the other omitted resistor, R2, is only installed with the parity option.

R8. Insert and solder the 8-position DIP switch at location 7A. Orient the switch so that "ON" is to the right. The DIP switch solders directly to the board without a socket.

R9. Install and solder the 5 volt 7805 regulator and 6106-14 heat sink (the larger of the two heat sinks) at location Q4. Neatly bend the regulator leads so they will route over the edge of the heat sink and down through the holes in the PC board without touching the heat sink or each other. Insert the regulator leads into the PC board holes and then attach the regulator and heat sink to the board with a 6-32x3/8" machine screw so that the following order results from bottom to top: machine screw head, PC board, heat sink, regulator, lock washer and nut. Before tightening the machine screw, position the heat sink regulator assembly as far as possible from the edge of the PC board. Finally, solder the regulator leads.

R10. Install and solder the 12 volt 7812 regulator and 6107-14 heat sink at location Q3. Follow the procedure of the previous step.

R11. Insert and solder the 79L05 regulator at location Q1, orienting the regulator so that the flat edge corresponds to the flat edge indicated on the layout legend.

R12. Insert and solder the following tantalum capacitors, being careful to insert the + lead of each capacitor into the hole marked "+" on the layout legend. The + lead is sometimes indicated by a red dot on the capacitor. Refer to the

Assembly Information section for capacitor installation procedures.

Capacitor	Value	Location
( ) C1	2.2uF	ØA
( ) C2	2.2uF	ØA
( ) C3	6.8uF	ØB
( ) C4	6.8uF	ØB
( ) C5	6.8uF	ØD
( ) C6	6.8uF	ØD
( ) C11	6.8uF	8A

R13. Insert and solder the following capacitors:

Capacitor	Value	Location	Type
( ) C7	.ØØ47uF	1A	dipped mylar
( ) C8	1ØØpF	1C	dipped mica
( ) C9	.ØØ47uF	2A	dipped mylar
( ) C12	47pF	2E	ceramic disk
( ) C13	47pF	12E	ceramic disk
( ) C14	47pF	12E	ceramic disk

R14. Insert and solder the sixty .Ø47uF ceramic disk capacitors at the 6Ø locations marked on the layout legend with asterisks.

R15. Save the remaining 33pF capacitor (C1Ø) for special DMA applications. See the Special DMA Applications section for details.

R16. Be sure the computer power is off and then insert the RAM-16-A board into the computer motherboard. Now turn on the power and check for the following voltages across each indicated pair of capacitor leads:

Capacitor	Voltage
( ) C5	+5V ±5%
( ) C3	+12V ±5%

Turn off the computer power. If any of the voltages are not correct, then locate and correct the problem before proceeding.

R17. Install the delay line module in the socket at location 5A. Orient the delay line so that pin 1 (indicated by a dot or "IN") is inserted in pin 1 of the socket.

R18. Install the 28 TTL integrated circuits (all but the memory IC's). Be careful to orient each IC so that pin 1 is

inserted into pin 1 of the socket.

	Location	IC
( )	1A	74LS123 (or 74123)
( )	1B	74LS13
( )	1C	74LS132
( )	1D	74LS14
( )	2A	74S175
( )	2B	74LS00
( )	2C	74LS14
( )	2D	74S74
( )	3B	74LS08
( )	3C	74LS132
( )	3D	74LS352
( )	4A	7402
( )	4B	74S30
( )	4C	74LS02
( )	4D	74LS352
( )	5B	74S113
( )	5C	74LS393
( )	5D	74LS352
( )	6A	74S138
( )	6B	74LS75
( )	6C	74LS74
( )	6D	74LS30
( )	7B	74S00
( )	7C	74LS00
( )	8A	74S10
( )	8C	74S10
( )	8D	74LS241
( )	17E	74LS373

R19. Carefully following the MOS device handling procedures described in the Assembly Information section, install the thirty-two 4027 memory IC's. Be careful to orient each memory IC so that pin 1 is inserted into pin 1 of the socket. Since the capacitors cause a tight fit, it is easier to insert rows B and C before rows A and D.

R20. Inspect the PC board to see that all the IC pins are properly inserted into the socket holes. Check that no pins are bent under the IC, and that no pins are outside the socket.

R21. If you are assembling the RAM-16-A board for use with the HORIZON computer, install the three "G" jumpers at locations 2E, 5E, and 6E by soldering with a piece of resistor snipping. If you have a different computer, it is strongly recommended that bus pins 20, 61, and 70 (if not used for other purposes) be connected to ground on the motherboard so that the "G" jumpers may be used on the RAM-16-A board. If all three jumpers cannot be used, use as many as possible.

Connecting these pins to ground will help reduce excessive ground noise on some S-100 computers.

R22. Configure the 14-pin DIP header for location 7D as follows:

A. Connect pin 1 to pins 2 and 3.

B. Connect pin 6 to pin 7.

This configuration of the header is for use of the RAM-16-A board with a Z80 or Z80A microprocessor in an application where bank switching is not needed. For 8080 and/or bank switching use, configure the header as described in the Configuration and Using Bank Switching sections.

R23. If this board is to be used with a processor board which sources POC/ (bus pin 99) as an indication that the processor is being reset (e.g., North Star, Imsai, Vector Graphics, Processor Technology) then skip this step. For use with other processors (e.g., Altair 8800), cut the trace connecting 3C pin 5 with 3C pin 4 on the solder side of the board, and add a jumper between PRESET/ (bus pin 75) and 3C pin 4 on the component side of the board.

The assembly of the RAM-16-A board (less parity option) is now complete. Proceed to the checkout section.

RAM BOARD CHECKOUT

The following checkout procedure should be followed for a newly assembled board. It can also be used to diagnose problems in previously operational boards.

The following terms are used in specifying expected test results:

GND	ground, Ø volts DC
LOW	logic zero, Ø-.7 volts, normally about .3 volts
HIGH	logic one, 2.4-5.Ø volts, normally about 3 volts
+5V	+5 volts from power supply
AC	Signal with pulses (as opposed to DC signal)

When referring to the name of a signal from the schematic drawings, if the signal is identified with a bar over its name, then the name is followed by a slash (e.g., STORE/) in the checkout instructions. When describing an AC pulse, the notation ($\pm$W,P) refers to a positive or negative pulse with a width of W appearing with a period of P. For example, a positive pulse with width 12Ø nanoseconds appearing every 25 microseconds would be described as (+12Øns,25us). See Appendix 1 for details on how to detect pulse signals.

If an oscilloscope will be used to test the board, a "scope gound" may be installed by soldering a "bridge" of jumper wire between two of the three PC board holes that connect edge connector pins 5Ø and 1ØØ near location 13E. Note that either of the two regulator machine screws can also be used for ground test points.

C1. If your S-1ØØ bus computer has a control panel, then check out control panel operation of the RAM-16-A as described in this step. Otherwise, skip to step C2.

   A. Set the address select switches for the region where the RAM-16-A will be used (refer to the Configuration section for details).

   B. With the computer power off, install the RAM-16-A board into the motherboard.

   C. Using the control panel, attempt to deposit the zero value in the first byte of each 4K address region on the board. Then examine these addresses. If the values examined are not all zero, then skip to step C3. Otherwise, continue at step C2.

C2. If you do not already have a working computer, then skip to step C3. Otherwise, set the address select switches for an available 16K address region (see the Configuration section). Then, with the computer power off, install the RAM-16-A board into the computer motherboard. Now use a

memory test program to verify correct operation of the board. If you do not have a memory test program (such as the TM command in the North Star Monitor), then use the program listed in Appendix 2.

If the RAM-16-A does not fail the memory test after several hours of operation, then the board is operational and you may skip the remaining checkout steps. If systematic data or addressing errors are detected, then refer to the schematic drawings to diagnose and correct the problem. (The correspondence between addresses and RAM chips is given in Appendix 3.) If the RAM-16-A does not operate at all, then continue with step C3.

C3. Set the address switches labeled "2" and "3" on the DIP switch (2nd and 3rd from the top) to the "ON" position. The other six switches should be OFF. With the computer power off, install ONLY the processor board and the RAM-16-A into the computer motherboard. Turn on the power and depress and hold down the computer reset switch so that no memory requests are being made.

A. Check the following memory cycle request signals while the computer reset switch is depressed:

Signal	Location	Description
STORE/	4B pin 5	HIGH
INSTRUCTION-FETCH/	4B pin 11	HIGH
FETCH/	4B pin 6	HIGH
RUNNING-REFRESH/	6C pin 6	HIGH
DEPOSIT-CY/	4B pin 4	HIGH

If the signals are not as listed then refer to the schematic drawings and trace backwards to locate and correct the problem.

B. WAITING-REFRESH cycles should occur approximately every 25 microseconds. In the following table, let T refer to the period of PHI 2 in your computer (e.g., 250ns with a 4MHz processor and 500ns with a 2MHz processor). Check the following signals while the computer reset switch is depressed:

Signal	Location	Description
WRF	2A pin 3	AC, (+T,25us)
WAITING-REFRESH/	1C pin 12	AC, (-T,25us)
CYCLE-START	4B pin 8	AC, (+T,25us)
delay tap T1	5A pin 12	AC, (+T,25us)
delay tap T2	5A pin 4	AC, (+T,25us)
delay tap T3	5A pin 10	AC, (+T,25us)
delay tap T4	5A pin 6	AC, (+T,25us)

delay tap T5	5A pin 8	AC, (+T,25us)
CYC-END/	8C pin 6	AC, (-T-135ns,25us)
RAS-A/	9A pin 4	AC, (-T-40ns,25us)
RAS-B/	9B pin 4	AC, (-T-40ns,25us)
RAS-C/	9C pin 4	AC, (-T-40ns,25us)
RAS-D/	9D pin 4	AC, (-T-40ns,25us)
chip address bit 0	9A pin 5	AC, see note
chip address bit 1	9A pin 7	AC, see note
chip address bit 2	9A pin 6	AC, see note
chip address bit 3	9A pin 12	AC, see note
chip address bit 4	9A pin 11	AC, see note
chip address bit 5	9A pin 10	AC, see note

Note: Sometimes (+T,25us) and sometimes (+T-90ns,25us)

If the signals are not as listed, then refer to the schematic drawings and trace backwards to locate and correct the problem.

C4. Use the same setup as step C3. If the computer includes an auto-jump capability, then it should be set to jump to some address outside of the range 2000 hex through 5FFF hex (for example, E800 hex or 0). If the processor board has a PROM option at address 0, it should be disabled for this step. With the computer power on, depress and release the reset switch. The processor should repeatedly execute RST 7 instructions (FF hex) from address 38 hex. This should cause memory store requests to all addresses (resulting from the RST instruction stack pushes). Check the following signals:

Signal	Location	Description
INSTRUCTION-FETCH/	4B pin 11	AC, (-220ns,11T)
FETCH/	4B pin 6	AC, see note 1
STORE/	4B pin 5	AC, (-220ns twice,11T)
RUNNING-REFESH/	6C pin 6	AC, (-260ns,11T)
RAS-A/	9A pin 4	AC, see note 2
RAS-B/	9B pin 4	AC, see note 2
RAS-C/	9C pin 4	AC, see note 2
RAS-D/	9D pin 4	AC, see note 2
chip write enable	9A pin 3	AC, (-220ns twice,11T)
CAS-A/	9A pin 15	AC, (-210ns thrice,11T)
CAS-B/	9B pin 15	AC, (-210ns thrice,11T)
CAS-C/	9C pin 15	AC, (-210ns thrice,11T)
CAS-D/	9D pin 15	AC, (-210ns thrice,11T)

Note 1: (-100ns,11T) with Z80A, (-210ns,11T) with 8080.

Note 2: Sometimes (-225ns,11T) and sometimes (-225ns twice,11T).

If the signals are not as listed, refer to the schematic

drawings to locate and correct the problem.

C5. This step will test the memory fetch and store operations by forcing the computer to execute alternating RST 7 and MOV A,A instructions repeatedly.

A. Set the address select switches labeled "1" and "2" on the DIP switch (1st and 2nd from top) to the ON position. The other six switches should be OFF.

B. With the power off, remove the 74LS373 IC from location 17E of the RAM board. (This disconnects the RAM-16-A from the DI bus.)

C. With a piece of jumper wire, make a temporary solder connection between 17E pin 15 (DI7) and 5D pin 6 (AØ) on the solder side of the RAM-16-A.

D. If the processor board has a PROM option, it should be disabled for this step.

E. With the power off, install ONLY the processor board and the RAM-16-A board in the computer motherboard.

F. Turn on the computer power. The repeated executions of the RST 7 instruction should fill the entire RAM-16-A board with alternating bytes containing 3A hex and ØØ (resulting from the stack pushes of the RST instruction).

G. Check the following signals at the memory chip at location 1ØD:

Signal	Location	Description
Vbb	1ØD pin 1	-5V
DI	1ØD pin 2	mostly HIGH, LOW during first PWR
WE/	1ØD pin 3	AC, two pulses, one during each PWR
RAS/	1ØD pin 4	AC, see note 1
AØ/	1ØD pin 5	AC, see note 2
A2/	1ØD pin 6	AC, see note 2
A1/	1ØD pin 7	AC, see note 2
Vdd	1ØD pin 8	+12V
Vcc	1ØD pin 9	+5V
A5/	1ØD pin 1Ø	AC, see note 2
A4/	1ØD pin 11	AC, see note 2
A3/	1ØD pin 12	AC, see note 2
CS/	1ØD pin 13	GND
DO	1ØD pin 14	AC, see note 3
CAS/	1ØD pin 15	AC, see note 4
Vss	1ØD pin 16	ØV

Note 1: Usually four pulses per loop (15T or 16T), two at M1 leading edges for fetches; two at M1 trailing edges

for refresh. Occasionally two more during stores.

Note 2: Signal is complicated, with many transitions per loop.

Note 3: Rises during one SM1 pulse, falls during the next, alternately. Additionally, for those stores that actually reference the chip (1/16 of the stores), the signal goes LOW during the first store and HIGH during the second.

Note 4: Four pulses per loop, two fetches and two stores.

H. Check the following data output signals on the RAM-16-A. If you are using an oscilloscope, then trigger on 1D pin 11 or the upper end of R1Ø at 12E (SM1) on the RAM-16-A.

Signal	Location	Description
MD5	1ØA pin 14	AC, see note 3 above
MD4	11A pin 14	AC, see note 3 above
MD6	12A pin 14	see note 5 below
MD1	13A pin 14	AC, see note 3 above
MDØ	14A pin 14	see not 5 below
MD2	15A pin 14	see note 5 below
MD3	16A pin 14	AC, see note 3 above
MD7	17A pin 14	see note 5 below

Note 5: Mostly low, high during store cycles outside of the address range of the board.

I. Replace the 74LS373 at location 17E, replace the 74LS28Ø at location 1ØE if it was removed, remove the jumper wire, and re-enable the processor board PROM option if it was disabled.

PARITY OPTION ASSEMBLY AND CHECKOUT

Skip this section if you did not purchase a parity option (RAM-16-PAR) for your RAM-16-A board. If you are installing the parity option, first be sure the board is completely checked out without the parity option.

P1. Insert and solder the five 16-pin IC sockets at locations 3A, 9A, 9B, 9C, and 9D, referring to the Assembly Information section for correct installation procedure. Orient the sockets so that pin 1 of each socket is inserted into the hole marked for pin 1 on the layout legend.

P2. Insert and solder the two 14-pin sockets at locations 10E and 15E. Also, insert and solder the 8-pin socket at location 0A. Be sure that the orientation is correct.

P3. Insert and solder the following resistor, referring to the Assembly Information section for correct resistor installation procedures.

	Resistor	Value	Size	Location	Color-code
( )	R2	220	1/4W	0B	red-red-brn

P4. Insert and solder the LED indicator near location 1A. The edge of the red plastic bulb of the LED near one of the two leads is either flat or notched. The LED should be oriented so that this lead is towards the left (nearest C2). For best visiblity when the board is mounted in the computer, bend the leads so that the LED lies parallel to the board, pointing towards the top of the board.

P5. Add a jumper to the DIP header at location 7D from pin 4 to pin 8. This selects bit 6 as the parity control bit for the memory board. See the Configuration section for details.

P6. Insert the four TTL integrated circuits. Be sure that pin 1 of each IC is inserted into pin 1 of its socket.

	Location	IC
( )	0A	75452
( )	3A	74LS109
( )	10E	74LS280
( )	15E	74LS280

P7. Using the MOS device handling procedures described in the Assembly Information section, install the four memory IC's in locations 9A, 9B, 9C, and 9D. Be sure that pin 1 of each memory IC is inserted into pin 1 of its socket.

P8. Visually inspect the PC board to see that all the IC pins

are properly inserted into the IC sockets. Check that there are no pins outside the sockets and that there are no pins bent under the IC's.

P9. Configure the RAM board with all the address switches OFF. Install the RAM board in the computer and then turn on the power and depress and release the reset switch. The LED should NOT be lit. If it is, turn off the computer and locate the problem before proceeding.

P1Ø. Select an unused address region in your computer and configure the address switches on the RAM board for that region. Plug the board in and turn on the computer power. Do not execute any software which initializes the RAM board. [E.g., the HORIZON DOS will initialize all RAM in the computer. To bypass this, boot up with only 8K of the board (addressed at 2ØØØH) turned ON, and turn on the other 8K after boot load.] Next, examine cells in the address region of the memory board using a monitor program or control panel. Eventually, you will examine a cell which powered up with a parity error. When this occurs, the LED should light. Now turn off the computer power. If the LED did not light, then locate and correct the problem before continuing.

P11. Power up the computer with the RAM-16-A board installed in the motherboard. Use a program such as the standard HORIZON DOS initialization to store into each byte on the board, to clear all incorrect parity bytes. Again, enable the parity detection by executing the two instructions shown in the previous step. (It is normal for the LED to turn on momentarily during this sequence: it should turn off when the arming instruction is executed.) It should not now be possible to turn on the LED by examining cells on the RAM board. If the LED does turn on, then either the memory is making errors or there is a problem with the parity option. Locate and correct the problem before continuing.

The parity option is now assembled and checked out.

CONFIGURATION

This section describes each of the RAM-16-A options which must be configured before use of the RAM-16-A. Note that configuration of the parity logic and bank switching logic is described in later sections.

ADDRESS SELECTION

Address selection for the RAM-16-A is determined by the switches at location 7A. To configure the RAM-16-A for a contiguous 16K byte region of addresses beginning at an 8K boundary, two adjacent switches should be ON (right side depressed) and the other six switches should be OFF (left side depressed), according to the following table:

Address Region	Switches on
0000-3FFF	1 and 2 (1st and 2nd)
2000-5FFF	2 and 3 (2nd and 3rd)
4000-7FFF	3 and 4 (3rd and 4th)
6000-9FFF	4 and 5 (4th and 5th)
8000-BFFF	5 and 6 (5th and 6th)
A000-DFFF	6 and 7 (6th and 7th)
C000-FFFF	7 and 8 (7th and 8th)

Note: Certain pairs of non-adjacent 8K address regions starting on 8K boundaries can be selected if, using the following table, exactly one switch is ON from each column:

Region	Switch	Region	Switch
0000-1FFF	1 (1st)	2000-3FFF	2 (2nd)
4000-5FFF	3 (3rd)	6000-7FFF	4 (4th)
8000-9FFF	5 (5th)	A000-BFFF	6 (6th)
C000-DFFF	7 (7th)	E000-FFFF	8 (8th)

Z80 OR 8080 COMPATIBILITY

The RAM-16-A must be configured to specify whether it is being used with a Z80 or 8080 microprocessor. Connect pin 1 to pin 2 on the DIP header at location 7D if Z80 or Z80A operation is required. Do not connect pins 1 and 2 if 8080 operation is required. (Note that pin 1 should be connected to pin 3 in either case, if bank switching will not be used.)

SIGNAL GROUNDING

It is strongly recommended that bus pins 20, 61, and 70 be connected to ground on the computer motherboard. Some S-100 computers (e.g., the HORIZON) already do this. For each of the three bus pins that are connected to ground, connect the appropriate "G" jumper on the RAM-16-A. The "G" jumpers are

located at positions 2E, 5E, and 6E.

PHANTOM MEMORY

The RAM-16-A board can be used with some area of ROM superimposed over the address region of the board. If the PH jumper (near location 4E) is installed, then a memory reference to the board will be inhibited if the backplane signal PHANTOM (motherboard pin 67) is LOW. Do not connect the PH jumper unless you intend to use this feature.

USING THE PARITY OPTION

PARITY ERROR ACTION

The action taken when a parity error occurs (when armed) is determined by connecting a jumper wire between "PE" (near location 3E) and one of the following labeled locations:

PINT/ Causes an interrupt request in systems not using vectored interrupts.

NMI/ Causes a non-maskable interrupt request in Z80 computers.

VI0/-VI7/ Connecting to one of these eight locations causes a vectored interrupt request at the corresponding priority level.

Note: The on-board LED lights whenever a parity error is detected, whether armed or not.

PARITY ERROR ARMING

The parity error logic is disarmed at power-on and reset. The parity error logic can be armed or disarmed under program control by loading a control value into the A-register and executing an OUT 0C0H instruction. Bit 0 of the control value should be 1 to arm the parity logic and 0 to disarm it. Configuration of the DIP header at location 7D will determine which bit (of bits 1-7) in the control value, if 1, will cause arming or disarming of the parity logic for the RAM-16-A. (Arming or disarming the parity error logic also resets the parity error flip-flop.)

Parity Select Bit	Header Connection
Bit 1	pin 4 to pin 14
Bit 2	pin 4 to pin 11
Bit 3	pin 4 to pin 9
Bit 4	pin 4 to pin 12
Bit 5	pin 4 to pin 10
Bit 6	pin 4 to pin 8 (standard)
Bit 7	pin 4 to pin 13

Note that the standard HORIZON convention is to use bit 6 for all RAM-16-A boards in the computer. Using this convention, the following two instructions will reset then arm the parity logic for all the RAM boards:

```
MVI A,41H
OUT 0C0H
```

and the following two instructions will reset and disarm the

parity logic:

```
MVI A,40H
OUT 0C0H
```

After power-on, the memory bytes will contain random values (including the parity bit), and not all bytes will have correct parity. Before arming the parity logic, clear all bytes to correct parity by storing into all bytes of RAM. Note that the standard HORIZON DOS initialization performs this function.

USING BANK SWITCHING

At any time, a RAM-16-A may be in one of two "states":

ON — In this state the board will respond to memory references made to the addresses specified by the address selection switches.

OFF — In this state the board will ignore all memory references from the processor. However, all values on the board will be retained, and refresh cycles will continue.

Thus, it is possible for more than one board to share the same address region in the computer. However, for any particular address region, at most one RAM-16-A should be ON at any given moment.

Configuration of the DIP header at location 7D determines if the board powers up in the ON state (connect pin 6 to pin 7) or in the OFF state (connect pin 5 to pin 6).

The RAM-16-A can be turned on or off under program control by loading a control value into the A-register and executing an OUT ØCØH instuction. Bit Ø of the control value should be Ø to turn the board ON and 1 to turn the board OFF. Configuration of the DIP header at location 7D will determine which bit (of bits 1-7) of the control value, if 1, will cause the board to be set:

Select Bit	Header Connection
Bit 1	pin 3 to pin 14
Bit 2	pin 3 to pin 11
Bit 3	pin 3 to pin 9
Bit 4	pin 3 to pin 12
Bit 5	pin 3 to pin 10
Bit 6	pin 3 to pin 8
Bit 7	pin 3 to pin 13

THEORY OF OPERATION

The RAM-16-A consists of a 4 by 8 (4 by 9 if parity is included) array of 200ns 4K dynamic 4027 RAM chips plus additional circuitry which performs the necessary support functions. Refer to the schematic drawings while reading the following theory of operation.

TYPES OF CYCLES

THE RAM-16-A employs three types of cycles in its operation. In each case the cycle is initiated by the CYCLE-START signal which is passed through the tapped delay module to provide the cycle timing.

1. Normal memory cycles are RAS,CAS cycles, which use A5-A0 as row address bits, then A11-A6 as column address bits. If the signal WE is asserted, a store cycle is performed, otherwise a fetch cycle is performed.

2. Deselect cycles are CAS-only cycles, performed during normal memory cycles on all BUT the selected chips. The CAS without a preceding RAS turns off the output drivers so as not to interfere with the data from the selected chips.

3. Refresh cycles are RAS-only cycles, performed by all chips on the board simultaneously. The row address comes from the 74LS393 refresh counter.

CYCLE TIMING

The following is the nominal (disregarding gate delays) timing for a normal memory cycle with respect to CYCLE-START:

Time	Event
0ns	Begin cycle, allow address and control signals to stabilize.
35ns	Begin RAS pulse to selected chips.
60ns	Switch address multiplexers to column inputs.
110ns	Begin CAS pulse to all chips.
215ns	Begin CYC-END pulse.
245ns	Terminate RAS.
320ns	Terminate CYC-END, terminate CAS.

CONDITIONS LEADING TO CYCLE START

1. The INSTRUCTION-FETCH flip-flop is set by the leading edge of SM1. For a Z8Ø processor, the instruction fetch presents the tightest access time requirement (even though SM1 precedes SMEMR).

2. For a Z8Ø processor, the FETCH flip-flop is set by the leading edge of SMEMR.

3. For an 8Ø8Ø processor, the FETCH flip-flop is set by the AND of PSYNC, PHI 1, and D7 which is an anticipation of MEMR status.

4. Note that it is possible to have INSTRUCTION-FETCH and FETCH set simultaneously, a condition which is redundant but harmless.

5. The STORE flip-flop is set by the leading edge of PWR unless blocked by SOUT. STORE causes a CYCLE-START and a WE.

6. A control panel deposit is detected as the AND of MWRITE and SMEMR, which causes first a DEP-RQ and then a DEPOSIT-CY. The deposit cycle is delayed if it would otherwise immediately follow a waiting refresh cycle.

7. The RUNNING-REFRESH flip-flop is set by the trailing edge of SM1 and provides refresh cycles when the processor is running. As long as there are 64 instructions executed in any 2ms period, this type of cycle will satisfy the refresh requirements.

8. Whenever 2Øus (approximately) elapses with no cycles of any kind, the retriggerable one-shot RECENT goes false, allowing a WAITING-REFRESH cycle. This type of cycle therefore maintains refresh activity when the reset switch is depressed, during long wait states (control panel or North Star disk controller), or when an 8Ø8Ø is halted. See the next section for more information.

NOTES ON WAITING-REFRESH

1. The WAITING-REFRESH flip-flop is clocked on the trailing edge of the PHI 2 clock, and is true for only one clock period.

2. The refresh cycle is delayed by a DEP-REQ if a control panel deposit cycle is in progress or will start on the next clock cycle. A refresh and a deposit cycle cannot occur on the same or sequential clock cycles.

3. Since some of its input conditions are asynchronous to the PHI 2 clock, the setup and hold times of the WAITING-REFRESH flip-

flop cannot be guaranteed to be met, and there is a small but finite chance that it will go into a momentary indecisive state. For this reason, a network of a resistor, capacitor, Schmitt inverter, and Schmitt gate filter the output to avoid the chance of sending an erroneous pulse down the delay module. Since a Schottky flip-flop is used, the filter slows down the signal by 10-15ns.

4. Whenever the processor resumes computation following a pause, refresh cycles must be inhibited lest one collide with the first memory cycle. The RAM-16-A recognizes three such cases:

   a. at the end of a wait state, the leading edge of PRDY or XRDY sets the WAIT-EXIT flip-flop, inhibiting refresh cycles. If this flip-flop initially comes up true, CLR will reset it.

   b. at the end of an 8080 halt phase (the Z80 maintains SM1 activity while halted) the trailing edge of SHLTA triggers the HLT/RST-EXIT one-shot, inhibiting refresh cycles for a few microseconds.

   c. at the end of a system reset, the trailing edge of POC or PRESET, if so jumpered, (whichever occurs last) triggers the same one-shot.

BOARD SELECT AND CHIP SELECT

The RAM-16-A occupies two 8K regions of a 64K byte address space. Address bits A15, A14, and A13 go to a one-of-eight decoder, the outputs of which go to eight switches. The switches are grouped by fours, with 1, 3, 5, and 7 connected together as BS-CD/ and 2, 4, 6, and 8 connected together as BS-AB/. The most common configuration would be to have two adjacent switches ON and the other six OFF. However, the two switches do not have to be adjacent, as long as one is connected to BS-AB/ and one to BS-CD/.

The board has four 4K regions corresponding to "lines" of chips labeled A, B, C, and D (one hesitates to call them "rows" or "columns" because that terminology is used to designate bit arrays within the chips). For a normal memory cycle, only one line should receive a RAS; other lines do a deselect (CAS-only) cycle. The line which is selected for a memory cycle is determined by combining BS-AB and BS-CD with address bit A12, while the RAS timing comes from the delay module. Note, however, that during a refresh cycle REF-SEL causes all four lines to receive a RAS but not a CAS.

Memory cycles to all four lines on the board are inhibited if OCCLUDE is true (see Bank Switching below), as none of the outputs of the decoder can go low. Similarly, if the PH jumper

is installed, all memory cycles are inhibited whenever the backplane signal PHANTOM (pin 67) is low. PHANTOM is used in some systems to superimpose a ROM over areas normally occupied by RAM.

BANK SWITCHING

Provision is made for a system with more than 64K bytes of memory by allowing more than one board to occupy a given address region, as long as only one board responds to any memory reference. This is accomplished by the flip-flop OCCLUDE which, if set, makes the entire board "invisible" to the processor.

The OCCLUDE flip-flop may be set or reset by an OUT instruction to port CØ hex. The port number is hardwired and may only be changed by rearranging the address inputs to the board. Data bit Ø goes to the D input of this flip-flop. The clock to the flip-flop may be gated by any of the other seven data bits (selection made by jumper). Thus, we have a theoretical maximum of seven "banks" of 64K, or 28 boards.

The CLR signal can initialize OCCLUDE either ON or OFF.

PARITY

The PARITY-ARM flip-flop is programmed in the same manner as OCCLUDE: its D input comes from data bit Ø and its clock can be gated via a jumper by any of the other seven data bits. The same pulse that clocks PARITY-ARM on its trailing edge clears the PARITY-ERROR flip-flop.

PARITY-ERROR is set during a memory fetch cycle if a byte with even parity is read and, via a driver, lights the on-board LED. The AND of PARITY-ARM and PARITY-ERROR goes to another driver, the output of which the user may wire to one of the eight vectored interrupts, to PINT, or to NMI.

The CLR signal initializes the PARITY-ERROR and PARITY-ARM flip-flops off.

SPECIAL DMA APPLICATIONS

This section describes modifications for the RAM-16-A which may be necessary for use with such DMA devices as the Cromemco DAZZLER™. These modifications are only needed if the RAM-16-A is being used with a Z80 or Z80A processor board. (To use the RAM-16-A with a special DMA device in an 8080-based system, it is necessary only to install a resistor as described in step D1 below.)

D1. If the DMA device is simulating an 8080 memory cycle, DO7 must be true during PSYNC. If the device does not drive DO7, a pull-up resistor (say, 1K) to Vcc will suffice. A logical place to add this resistor would be at the DMA controller.

D2. Install resistor R12 (220 ohm, red-red-brn) at location 5E and capacitor C10 (33pF dipped mica) at location 5E. This R-C circuit acts as a delay for the CC-DBSL/ signal.

D3. Add an unused inverter to the circuit by connecting a jumper wire between the location labeled PHLDA (location 7E) to 2C pin 11 and another jumper wire from 2C pin 10 to 2D pin 12. Now cut the trace from 2C pin 12 to 2C pin 10.

D4. Add a second inverter to the circuit by connecting a jumper wire from the location labeled CC-DSBL/ (location 4E) to 7C pins 4 and 5 and another jumper wire from 7C pin 6 to 7D pin 1. Also, cut the trace on the solder side of the PC board between 7D pin 1 and 7C pin 7. This allows memory cycles to start on the condition:

PSYNC AND PHI 1 AND CC-DSBL/

D5. On the header at location 7D, be sure the jumper from pin 1 to pin 2 is installed, as it should be for Z80 operation.

D6. Mark the changes on the schematic drawings.

APPENDIX 1. PULSE SIGNAL DETECTION

Some steps in the checkout procedure will require test equipment capable of distinguishing a signal containing pulses from a DC signal. Any one of the following will suffice.

1. Use of an oscilloscope is best since the shape and frequency of the pulses can also be determined.

2. Use a logic probe that detects pulses.

3. If the RAM-16-A is being assembled for use with a HORIZON, then use a counter on the motherboard to divide the frequencies down to the audio range and then play the result through a hi-fi amplifier. To do this, remove the 74LS161 at location 7D on the motherboard. Then attach the test probe wire to jumper 2D pin 16 (this is the input to the divider). Next, take the output of the divider at jumper 10A pin 11 and connect to the AUX input of the audio amplifier. Finally, connect the AUX input ground on the audio amplifier to signal ground on the motherboard. This arrangement will divide high frequency signals by 4096 and thus put the resulting signal in the audible range. Thus a 4 MHz signal will be heard as a tone one octave higher than a 2MHz signal.

4. Construct the "probe" shown in figure 1C on a piece of cardboard or perf-board. This probe converts high frequency signals to DC signals. The voltage of the resulting DC signal will be proportional to the duty factor of the tested wave form.

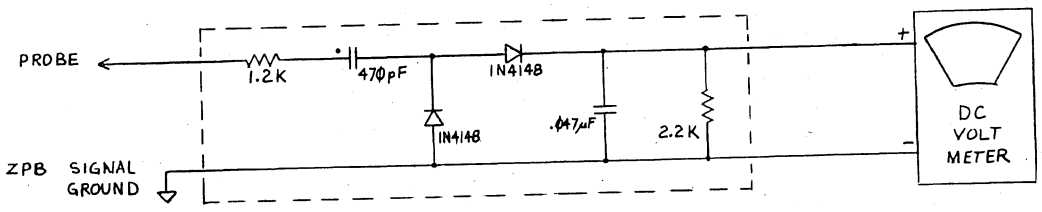


FIGURE 1C: A.C. SIGNAL DETECTOR

APPENDIX 2: MEMORY TEST PROGRAM

```
0000            *
0000            *SUBROUTINE TO TEST 4K BLOCK OF RAM
0000            * (MUST BE ORIGINED ON 256-BYTE BLOCK BOUNDARY)
0000            *
0000            *ENTER WITH BLOCK ADDRESS IN DE (MUST BE 4K BOUNDARY)
0000            *
0000            *NOTE THAT ERROR ACTION ROUTINE MUST BE SUPPLIED
0000            *
0000 01ED00     TB LXI B,PATTERN  LOAD B,C WITH PATTERN TABLE PTR
0003 60           MOV H,B         LOAD H WITH MSB OF PTR
0004 69         PASS MOV L,C      LOAD L WITH LSB OF PTR
0005            *  BEGIN WRITE FORWARD TO 4K RAM LOOP
0005 7E         WFL MOV A,M       LOAD A WITH NEXT BYTE OF PATTERN
0006 12           STAX D          WRITE IT TO RAM UNDER TEST
0007 2C           INR L           STEP PATTERN PTR
0008 C20E00       JNZ WFI         SKIP IF NOT AT END OF PATTERN
000B 21ED00       LXI H,PATTERN   RESET PATTERN TABLE PTR
000E 1C         WFI INR E         STEP RAM PTR
000F C20500       JNZ WFL         LOOP IF NOT AT 256 BOUNDARY
0012 14           INR D           STEP MSB OF RAM PTR
0013 7A           MOV A,D         TEST MSB OF PTR
0014 E60F         ANI 17Q         DONE FILLING 4K?
0016 C20500       JNZ WFL         LOOP IF NOT AT 4K BOUNDARY
0019 7A           MOV A,D         RESET 4K RAM PTR TO BEGINNING
001A D610         SUI 20Q         "     "     "     "     "
001C 57           MOV D,A         "     "     "     "     "
001D 69           MOV L,C         RESET PATTERN PTR
001E            *  BEGIN READ FORWARD AND COMPARE LOOP
001E 46         RFL MOV B,M       GET PATTERN VALUE
001F 1A           LDAX D          GET BYTE FROM RAM
0020 B8           CMP B           CMP BYTE WITH PATTERN
0021 C46700       CNZ ERROR
0024 2C           INR L           STEP PATTERN PTR
0025 C22B00       JNZ RFI         SKIP IF NOT AT END OF PATTERN
0028 21ED00       LXI H,PATTERN   RESET PATTERN TABLE PTR
002B 1C         RFI INR E         STEP RAM PTR
002C C21E00       JNZ RFL         LOOP IF NOT AT 256 BOUNARY
002F 14           INR D           STEP MSB OF PTR
0030 7A           MOV A,D         TEST MSB OF PTR
0031 E60F         ANI 17Q         DONE WITH 4K REGION?
0033 C21E00       JNZ RFL         LOOP IF NOT AT 4K BOUNDARY
0036            *  END OF READ LOOP
0036            *
```

```
0036           *
0036           *WE HAVE COMPLETED A READ AND WRITE PASS
0036           *NOW TEST BACKWARDS TO CATCH ADDRESSING ERRORS
0036
0036 69            MOV L,C         DECR RAM PTR
0037 1B        WBL DCX D           BEGIN BACKWARDS WRITE
0038 7E            MOV A,M         LOAD NEXT BYTE OF PATTERN
0039 12            STAX D          WRITE IT TO RAM
003A 2C            INR L           STEP PATTERN PTR
003B C24100        JNZ WBI         SKIP IF NOT AT END OF TABLE
003E 21ED00        LXI H,PATTERN   RESET PATTERN PTR
0041 7A        WBI MOV A,D         GET MSB OF PTR
0042 E60F          ANI 17Q         END OF 4K BOUNDARY?
0044 B3            ORA E           "     "     "
0045 C23700        JNZ WBL         LOOP IF NOT AT BLOCK BEGINNING
0048 7A            MOV A,D         RESET PTR TO END OF BLOCK
0049 C610          ADI 20Q         "     "     "     "
004B 57            MOV D,A         "     "     "     "
004C 69            MOV L,C         RESTORE TABLE PTR
004D 1B        RBL DCX D           READ PASS (BACKWARDS)
004E 46            MOV B,M         PATTERN
004F 1A            LDAX D          DATA
0050 B8            CMP B           COMPARE
0051 C46700        CNZ ERROR
0054 2C            INR L           STEP TABLE PTR
0055 C25B00        JNZ RBI         SKIP IF NOT AT END OF PATTERN
0058 21ED00        LXI H,PATTERN   RESET PATTERN TABLE PTR
005B 7A        RBI MOV A,D         STEP RAM PTR
005C E60F          ANI 17Q         BEGIN TEST
005E B3            ORA E           CONTINUE TEST
005F C24D00        JNZ RBL         LOOP IF NOT AT END OF 4K
0062 0C            INR C           CHANGE PATTERN
0063 C20400        JNZ PASS
0066 C9            RET             ALL DONE WITH TEST
0067           *
```

```
0067
0067          *ERROR ROUTINE (NOT SUPPLIED)
0067          * ON ENTRY, REGISTERS CONTAIN:
0067          *
0067          *  A  VALUE FOUND IN RAM
0067          *  B  VALUE SHOULD HAVE BEEN FOUND
0067          *  C  PASS NUMBER
0067          * DE  BAD BYTE ADDRESS
0067          * HL  ADDRESS OF PATTERN
0067          ERROR DS 206Q         PUT ERROR SUBROUTINE HERE
00ED
00ED          *  ADD YOUR ERROR ROUTINE HERE
00ED
00ED          *
00ED          *PATTERN TABLE
00ED
00ED 00       PATTERN DB 0
00EE 01          DB 1
00EF 02          DB 2
00F0 04          DB 4
00F1 08          DB 10Q
00F2 10          DB 20Q
00F3 20          DB 40Q
00F4 40          DB 100Q
00F5 80          DB 200Q
00F6 AA          DB 252Q
00F7 7F          DB 177Q
00F8 BF          DB 277Q
00F9 DF          DB 337Q
00FA EF          DB 357Q
00FB F7          DB 367Q
00FC FB          DB 373Q
00FD FD          DB 375Q
00FE FE          DB 376Q
00FF FF          DB 377Q         MUST BE END OF 256-BYTE BLOCK
0100          *
```

APPENDIX 3: ORGANIZATION OF RAM CHIP ARRAY

The organization of RAM chips on the PC board layout is as follows:

The row 10A-17A (9A-17A if the parity option is included) responds to the 4K area of addresses within the 16K region selected by the address select switches with first hex digit of 3, 7, B, or F. For example, if the RAM board select switches "2" and "3" are ON, then this row responds to addresses in the range of 3000-3FFF hex.

The row 10B-17B responds to the 4K area of the 16K address region with first hex digit of 2, 6, A, or E.

The row 10C-17C responds to the 4K area of the 16K address region with first hex digit of 1, 5, 9, or D.

The bottom row, 10D-17D responds to the 4K area of the 16K address region with first hex digit of 0, 4, 8, or C.

The columns of RAM chips each correspond to a different bit of each addressed byte:

The column 9A-9D contains the parity bit (if the parity option is included).

The column 10A-10D contains bit 5 (the 20 hex bit).

The column 11A-11D contains bit 4 (the 10 hex bit).

The column 12A-12D contains bit 6 (the 40 hex bit).

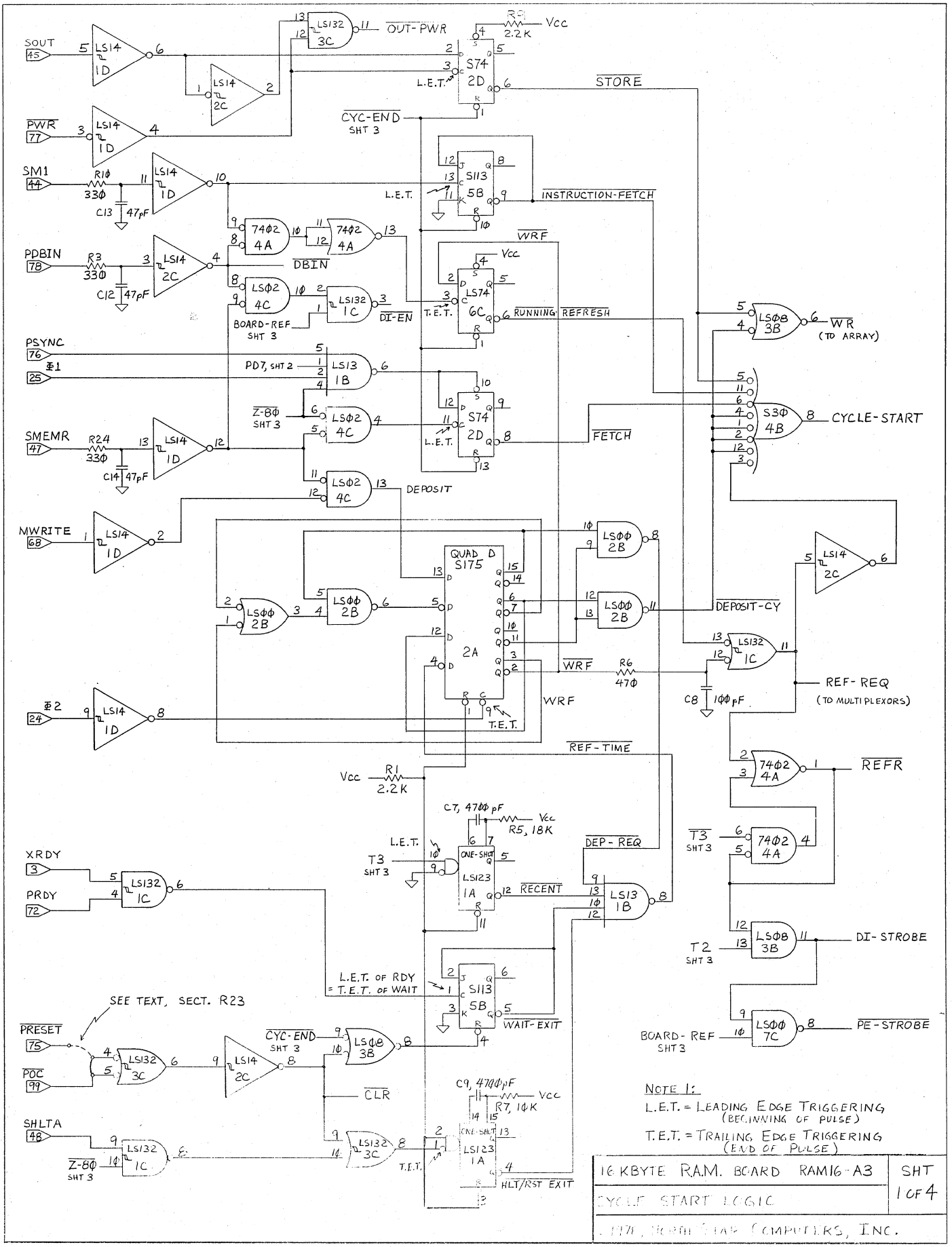
The column 13A-13D contains bit 1 (the 02 hex bit).

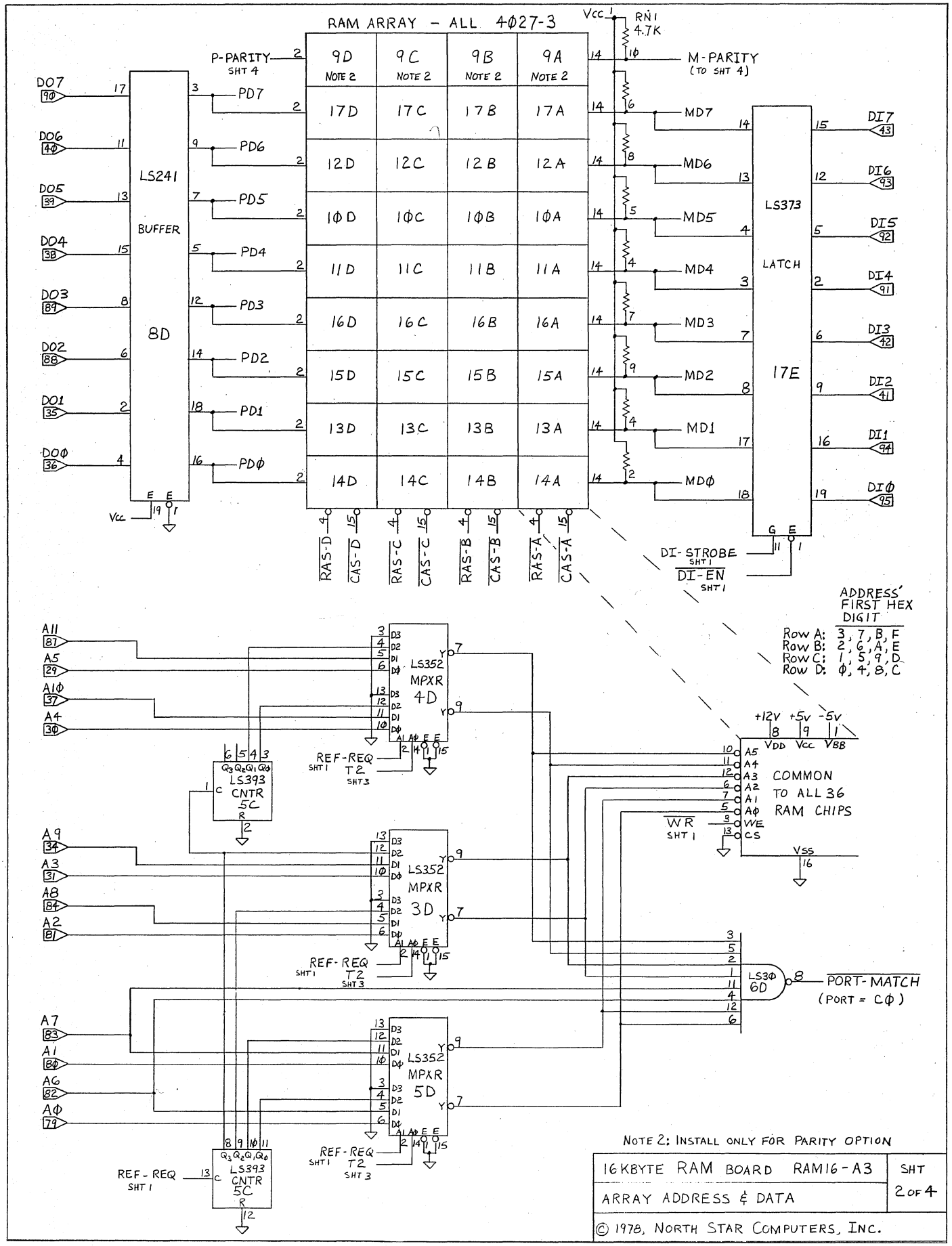
The column 14A-14D contains bit 0 (the 01 hex bit).

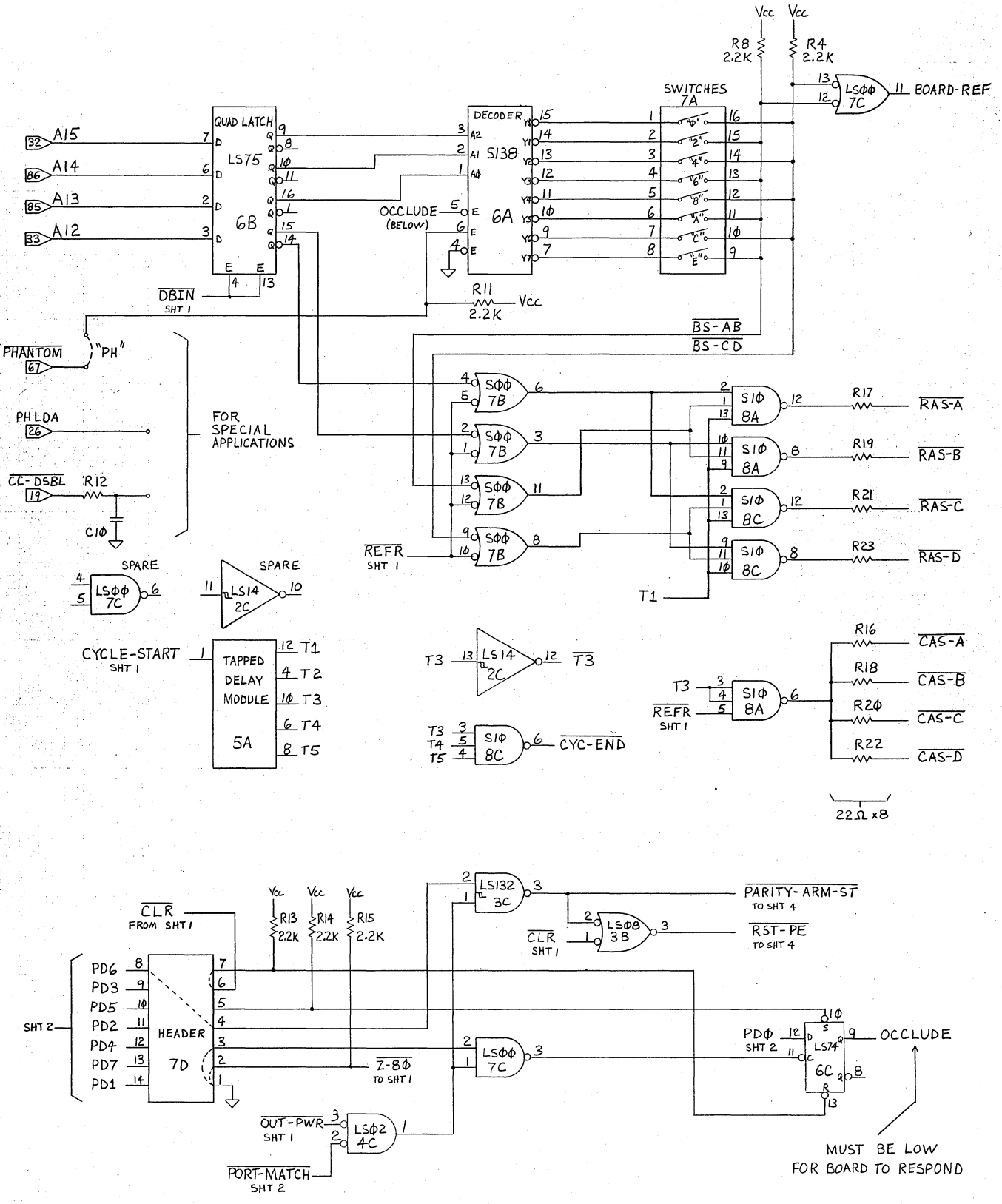
The column 15A-15D contains bit 2 (the 04 hex bit).

The column 16A-16D contains bit 3 (the 08 hex bit).

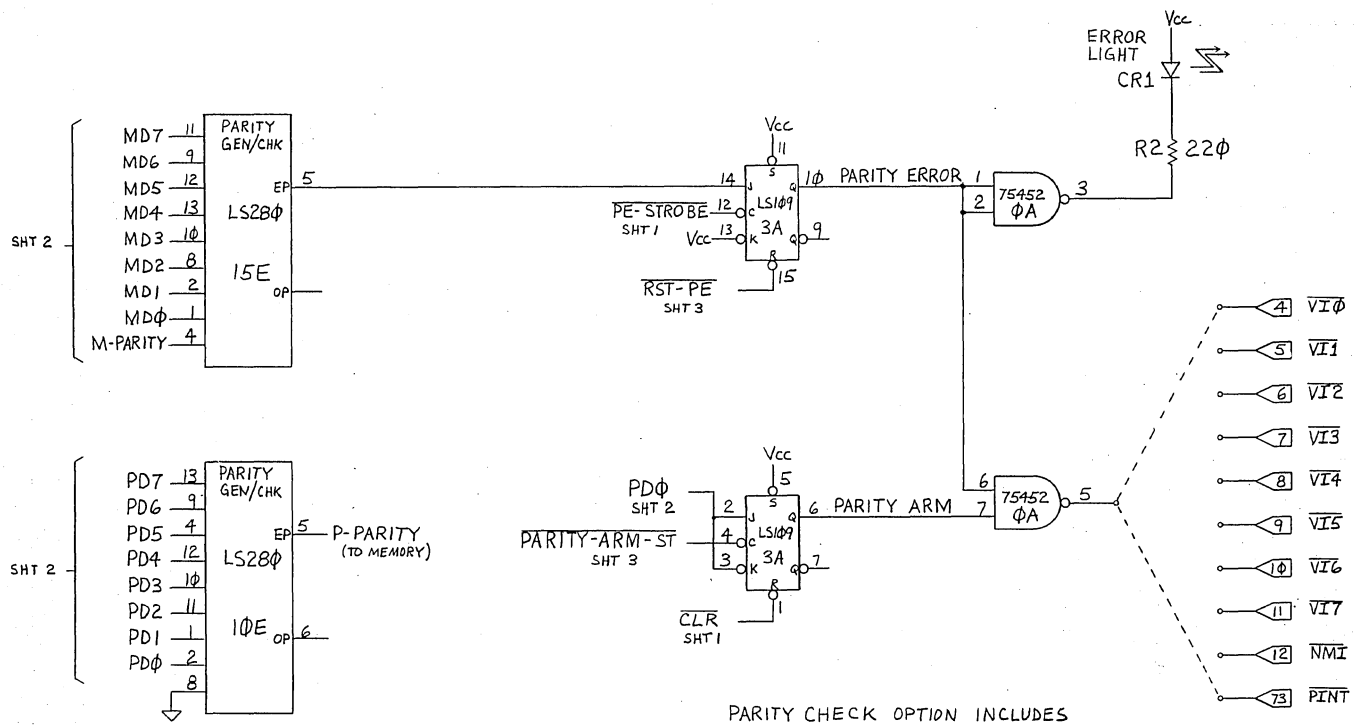
The column 17A-17D contains bit 7 (the 80 hex bit).


SOUT
PWR
SM1
PDBIN
PSYNC
SMEMR
MWRITE
Φ1
Φ2
XRDY
PRDY
PRESET
POC
SHLTA
OUT-PWR
STORE
CYC-END
SHT 3
INSTRUCTION-FETCH
WRF
DBIN
DI-EN
BOARD-REF
RUNNING
REFRESH
WR
(TO ARRAY)
CYCLE-START
FETCH
DEPOSIT
DEPOSIT-CY
REF-REQ
(TO MULTIPLEXORS)
REFR
REF-TIME
DEP-REQ
RECENT
WAIT-EXIT
DI-STROBE
PE-STROBE
HLT/RST EXIT
CLR
Z-BΦ
SHT 3
T3
SHT 3
T2
SHT 3
L.E.T.
T.E.T.
L.E.T. OF RDY
= T.E.T. OF WAIT
SEE TEXT, SECT. R23
QUAD D
S175
2A
ONE-SHOT
LS123
1A
Vcc
2.2K
330
47pF
47Φ
1ΦΦpF
R5, 18K
R7, 10K
NOTE 1:
L.E.T. = LEADING EDGE TRIGGERING
(BEGINNING OF PULSE)
T.E.T. = TRAILING EDGE TRIGGERING
(END OF PULSE)
16 KBYTE R.A.M. BOARD RAM16-A3
SHT 1 OF 4
CYCLE START LOGIC
1978, NORTH STAR COMPUTERS, INC.

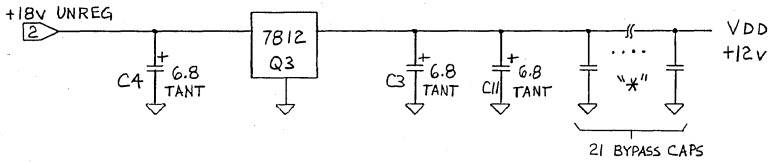

RAM ARRAY - ALL 4Ø27-3
9D NOTE 2
9C NOTE 2
9B NOTE 2
9A NOTE 2
17D
17C
17B
17A
12D
12C
12B
12A
1ØD
1ØC
1ØB
1ØA
11D
11C
11B
11A
16D
16C
16B
16A
15D
15C
15B
15A
13D
13C
13B
13A
14D
14C
14B
14A
P-PARITY SHT 4
M-PARITY (TO SHT 4)
RN1 4.7K
LS241 BUFFER 8D
LS373 LATCH 17E
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PDØ
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MDØ
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DIØ
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DOØ
RAS-D
CAS-D
RAS-C
CAS-C
RAS-B
CAS-B
RAS-A
CAS-A
DI-STROBE SHT 1
DI-EN SHT 1
ADDRESS FIRST HEX DIGIT
Row A: 3, 7, B, F
Row B: 2, 6, A, E
Row C: 1, 5, 9, D
Row D: Ø, 4, 8, C
LS352 MPXR 4D
LS352 MPXR 3D
LS352 MPXR 5D
LS393 CNTR 5C
REF-REQ SHT 1 T2 SHT 3
+12V +5V -5V
VDD Vcc VBB
COMMON TO ALL 36 RAM CHIPS
WR SHT 1
Vss
LSØØ 6D
PORT-MATCH (PORT = CØ)
NOTE 2: INSTALL ONLY FOR PARITY OPTION
16KBYTE RAM BOARD RAM16-A3
SHT 2 OF 4
ARRAY ADDRESS & DATA
© 1978, NORTH STAR COMPUTERS, INC.

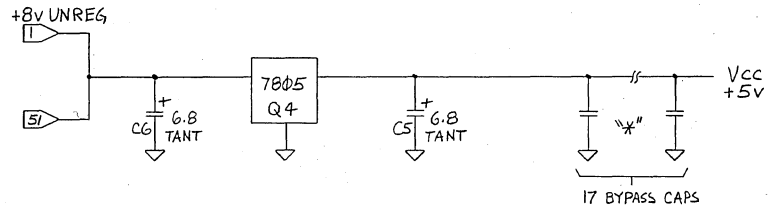


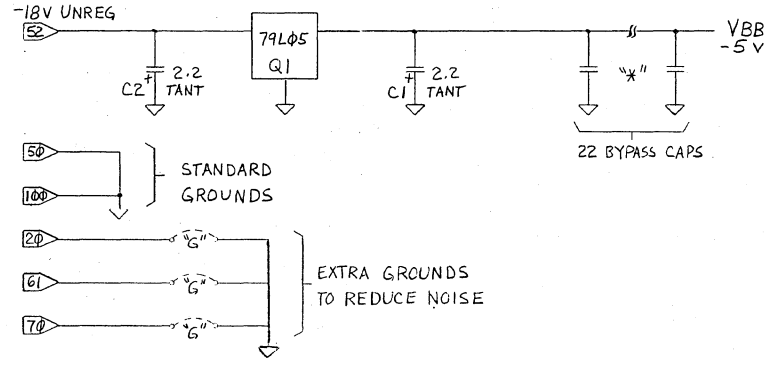
16 KBYTE R.A.M. BOARD RAM16-A3	SHT 3 OF 4
BOARD SELECT	



PARITY CHECK OPTION INCLUDES ABOVE LOGIC PLUS RAM CHIPS IN 9A, 9B, 9C, 9D







16KBYTE R.A.M. BOARD RAM16-A3	SHT 4 OF 4
PARITY CHECK OPTION, POWER	