IEEE 696/S-100

Modular Microcomputer Bus

A bus provides a defined set of paths for data, address, and control signals for a system. Additionally, provision must be made for power and any other utility signals a system may require. The IEEE 696/S100 proposed bus standard provides the definitions noted above in addition to defining bus signal timing and handshake conventions for DMA devices. The standard also specifies the form factor and dimensions of the S100 board. (See Appendix A, page 94). The form factor of the board which was originally produced by MITS in 1975 has been retained. This provides mechanical compatibility among boards produced by the hundreds of different manufacturers of S100 board products. Electrical compatibility is not as easily assured. Hopefully the outline of the electrical specification of the bus will aid the reader in design of new S100 products and evaluating existing products.

In the opinion of this writer, the systems architect for the S100 bus was not MITS but rather the designer of the Intel 8080. The logic signals present on the original bus are those of the 8080. The 8080 possesses many of the attributes of earlier large machines. The fortuitous result of this fact, whether by chance or design, is a logical structure which provides almost all of the control and status signals required for any microprocessor regardless of the size of data and address words. The influence of the 8080 has been so profound upon the design of later microprocessors that the IEEE 696/S100 bus can accommodate virtually any 8 or 16 bit processor. There are schemes under consideration for getting 32 bit machines on the bus sometime in the mid 80's.

The physical bus consists of 100 lines. These will be considered by function without regard to actual line or pin numbers. (See Appendix B, page 110, for actual pin assignments) All signal names which include reference to signal direction are made relative to the CPU or master, i.e. permanent master/"host processor" or temporary master such as a DMA device, whichever happens to be controlling the bus at the time the signal is referenced.

1. DATA 16 Lines

8 DI=Data In 8 DO=Data Out

In an 8 bit application the DO lines are usually driven by the bus master and the DI lines are driven by bus slaves such as memory or I/O. These lines are then considered uniderectional since data is always only received or transmitted on those lines by any particular board, master or slave. This mode of data transfer is also used by 16 bit processors such as the 8088 which performs 8 bit data transfers only. This transfer mode is also used by properly designed 16 bit CPU's when exchanging data with 8 bit slaves. Microprocessors such as the 8086 have both 8 bit and 16 bit transfer modes. The S100 bus contains provisions for signalling the bus master whether a particular device is capable of performing a 16 bit "word" transfer. If, for example, an I/O port is set up to handle only 8 bit "byte" transfers, then the 16 bit master should have a default mode which will perform 16 bit transfers in byte serial fashion. This means a system owner does not have to replace all the 8 bit memory and I/O in a system just to use a new 16 bit CPU.

In 16 bit applications the DO and DI lines are driven by both bus masters and slaves. The 16 data lines operate in a bi-directional mode. In this mode the 8 DO lines contain the least significant byte and the 8 DI lines contain the most significant byte. Word parallel data transfers are performed in this fashion between 16 bit masters and slaves. 16 bit slaves such as memory and I/O should include a default mode capable of performing byte serial transfers with 8 bit masters. The sections on Status and Control signals contain details about 16 bit transfers. 32 bit transfers could be accomplished between 16 bit devices by performing 16 bit word serial transfers.

2. ADDRESS 24 Lines
Memory 16/24 I/O 8/16

The 8080 and the original MITS bus provided only 16 address lines. Initially this was considered more than adequate. With the cost of RAM as high as it was, and in the virtually absence of software, 4K bytes were quite adequate and 8K bytes were heavenly! This state of affairs did not last for long. Many operating systems now occupy more than 16K and some interpreters require a minimum of 64K for proper operation. Multi user applications require considerably more. Initially an I/O scheme called "bank select" was devised to permit 8 bit processors to access more than the 64K which they could directly address. This scheme was cumbersome at best. The advent of newer MPU's with more than 16 address lines, v.g. the 8088 has 20, there was no need for bank select but the bus did need more address lines. The S100 standards committee added 8 address lines to the 16 already on the bus. The term IEEE extended addressing now refers to devices capable of decoding the full 24 bits of an address. The capability of directly accessing up to 16 Megabytes of RAM should fill just about any needs for the foreseeable future. All new designs should include extended addressing.

I/O addressing with the 8080 was 8 lines providing for up to 256 I/O devices. The proposed IEEE 696 contains extended I/O addressing using 16 lines to provide for up to 64K I/O devices. I/O addresses are asserted on the low order S100 address lines.

3. STATUS 8 Lines

The status lines are used to specify the type of bus cycle to be performed. Status should be asserted as early in a bus cycle as is possible. The first seven are 8080 originals; the last two are newly defined in IEEE 696.

A. sMEMR, status MEMory Read, is asserted whenever the current bus cycle is a memory fetch.

B. sM1, status Op-code fetch, is asserted along with sMEMR to identify a memory read cycle where the current bus master is calling an instruction from memory.

C. sINP, status INPut, is asserted whenever the current bus master is reading data from an I/O port.

D. sOUT, status OUTput, is asserted whenever the current bus master is writing data to an I/O port.

E. sWO*, status Write Out, is asserted whenever the current bus master is writing data to either memory or I/O.

F. sINTA, status INTerrupt Acknowledge, is asserted by the current bus master to indicate that it is prepared to service an interrupt request previously issued to it by a bus slave.

G. sHLTA, status HaLT Acknowledge, is asserted by the current bus master to acknowledge that a halt instruction has been executed.

H. sXTRQ*, status siXteen bit data Transfer Request, is asserted by the current bus master to ascertain if the currently addressed bus slave can perform 16 bit (word) transfers. If the request is not acknowledged by the slave the master should perform byte serial data transfers. This signal permits both byte and word organized slaves to operate on the same bus.

I. sMW, status Memory Write-a ninth status signal for which there is no bus line-is defined as sMW=(-sOUT).sWO.

4. Control Output 5 Lines

The control output signals establish the timing and movement of data during all bus cycles. These five are original 8080 signals. However, in the author's opinion there is a sixth signal, MWRT, memory write, which should have been included in this section of IEEE 696. This signal is covered in the utilities section of this

paper in order to maintain correspondence with IEEE 696. Designers and users should include MWRT in any consideration of timing and control relating to the S100 bus.

A. pSYNC, SYNChronize, indicates the start of each bus cycle.

B. pSTVAL*, STatus VALid (analogous to phi 1 on the 8080) signifies, in conjunction with pSYNC, that status and address are stable on the bus and ready for use. Proper assertion of pSTVAL requires that there be only one negative transition on pSTVAL during pSYNC.

C. pDBIN, Data Bus IN, is the general read strobe which gates data from an addressed slave onto the bus. Address signals must be held stable before, during and after assertion of pDBIN. Data from the slave must be stable on the bus sufficiently prior to the end of pDBIN to meet the read data access time requirements of the master asserting pDBIN.

D. pWR*, WRite, is the general write strobe which gates data from the bus into an addressed slave. Data and address signals must be held stable before, during and after assertion of pWR*.

E. pHLDA, HoLD Acknowledge, is asserted by the permanent bus master to indicate to the temporary master with highest priority that the permanent master is relinquishing control of the bus. Note that only the permanent bus master can issue pHLDA.

Timing diagrams of typical bus masters, an 8 bit Z80 and a 16 bit 8088, are contained on pages 232 and 233 of this manual.

5. Control Input 6 Lines

The control input signals provide the means by which bus slaves may synchronize bus masters with the timing requirements unique to the slaves. They also provide the means for slaves to request interrupt or hold operations from the permanent bus master.

A. RDY, ReaDY, is the general ready line for bus slaves. When not ready is asserted the bus master is stalled or caused to issue wait states until the slave removes the not ready signal. In this fashion slaves with slower access times than the bus masters can synchronize data transfers with those masters. RDY is an open collector line and should be terminated by an appropriate pull-up on the bus permanent master.

B. XRDY, eXternal ReaDY, is functionally redundant with RDY. XRDY is specified as a totem pole driven line so it cannot be used by more than one device without conflict. XRDY should not be used in new designs. XRDY was formerly used on the front panels of firms which are now defunct. The line was not deleted at the time IEEE 696 was originated because there were still a significant number of these front panels in use. The XRDY line is a candidate for future reassignment.

C. INT*, INTerrupt, is an open collector general interrupt service request line. The INT* line is often used with a slave device which services the 8 vectored interrupt lines defined in section 7. Interrupt requests are asserted on INT* as a level and when accepted by the bus master it will acknowledge with sINTA. INT* may be masked by internal software operations on the bus master.

D. NMI*, Non Maskable Interrupt, is An open collector interrupt service request line which cannot be masked of by the bus master. NMI* is asserted as a negative transition on the line and need not be acknowledged by a sINTA cycle.

E. HOLD*, HOLD request, is an open collector line used by temporary bus masters to request control of the bus. HOLD* may be software maskable by the Host Processor. HOLD* is acknowledged by an sHLTA cycle. Hold requests always take priority over interrupt requests. (See 7)

F. SIXTN*, SIXTeeN acknowledge, is an open collector signal line used by bus slaves to respond to sXTRQ* that 16 bit data transfers are possible. An absent or delayed SIXTN* should cause a bus master

to default to byte serial data transfer mode.

6. DMA Control 8 lines

DMA control is probably the least understood and most maligned part of IEEE/S100 specsmanship around. Well sports fans I'm sure that some of you have got your "skinnin knives" out by now and the rest of you poor souls who have worked your way through my stilted prose are just waiting to get in your shots. First, let me assure you that successful DMA design and operation are no more difficult than playing poker with some of the local fauna out here around Silicon Gulch. Some of the card sharks in the computer business make the Vegas kids look like slow third graders! So, what's the secret? First, you gotta know the rules, COLD. Second, you gotta know the odds, er, I mean priorities. Third, you must have good timing; ever try to run a bluff only to be murdered because your timing was bad? Proper timing in DMA operation is critical.

A. DMA0*, DMA1*, DMA2*, DMA3*, Direct Memory Access, 0 through 3 are open collector lines which carry the encoded priorities of up to 16 temporary bus masters. The priorities asserted on these lines are used to simultaneously arbitrate requests for bus control.

B. ADSB*, Address DiSaBle; DODSB*, Data Out DiSaBle; SDSB*, Status DiSaBle and CDSB*, Control DiSaBle; are open collector DMA control lines asserted by temporary bus masters to disable the address, data, status and control signals of the permanent bus master/Host Processor. also other bus masters ?

DMA operations are controlled by the 8 DMA control lines working in conjunction with HOLD* and pHLDA. A temporary master begins a DMA cycle by asserting HOLD*. It may do so ONLY when HOLD* and pHLDA are not true on the bus. No temporary master may request control when the permanent master is not in control of the bus. We shall assume that this HOLD request is the only one present on the bus. The Host Processor grants the request by asserting pHLDA. Only the permanent bus master/Host Processor may assert pHLDA. NESTED DMA OPERATIONS ARE NOT PERMITTED ON THE S100 BUS. The temporary master will continue to assert HOLD* until it relinquishes control of the bus to the Host Processor. Upon receipt of the bus grant, pHLDA, the temporary master asserts ADSB*, SDSB* and DODSB* while enabling its control outputs as shown below.

SIGNAL	LOGIC STATE
pSYNC	False
pSTVAL*	False
pDBIN	False
pWR*	False
pHLDA	True

The control signal outputs from both the Host Processor and the temporary master should match with both driving the bus.

The transfer between Host Processor and temporary master is completed by the temporary master asserting CDSB* and enabling its address, data and status outputs. Note the importance of overlapping drive on the control bus. pSYNC and pDBIN are active high signals. If the control signals were allowed to float for a few nanoseconds during transfer, one or more devices on the bus could see the slice (we are dealing with reasonably fast logic) and cause an unwanted reaction. Unwanted reaction is spelled CRASH or, worse yet, something so subtle that it does not appear until many lines of code have been executed. The control lines must not be allowed to float. Performing transfer of control as described above insures that the control lines will not float. The temporary master now has control of the bus. IEEE 696/S100 imposes no limit to the number of bus cycles a temporary master may perform before returning control to the Host Processor. This provides much flexibility for software system design. Transfer of system control from Host Processor to temporary master is called transfer state one, XS I. Transfer of system control from temporary master to Host Processor is called transfer state two, XS II. Performing the steps described for XS I in

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reverse order returns control of the bus to the Host Processor. A bus limited to one temporary master needs only control transfer logic.

The IEEE 696/S100 bus provides for a permanent master/Host Processor and up to 16 temporary masters on the same bus. The S100 DMA priority and bus arbitration protocol prevents contention between two or more temporary masters. DMA0* through DMA3* are the four lines which carry the priority information which controls the arbitration process. All temporary masters requesting a bus grant continuously sample the four DMA priority lines in parallel. Dot OR-ing active low priority outputs on the bus permits each requestor to simultaneously sample the bus and assert its priority. When disagreement occurs at any position the temporary master with lower priority disables all its less significant output bits. Temporary masters may assert their priorities and HOLD* request only when HOLD* and pHLDA are not asserted on the bus. Bus control is always given to the first requestor without regard to priority. The arbitration protocol comes into play only when more than one temporary master requests bus control. Arbitration logic on all temporary masters must be fast enough to insure completion of arbitration and bus settling time within the shortest period that can occur between assertion of Hold* and the response pHLDA.

7. VECTORED INTERRUPTS
8 Lines VI0 through VI7

IEEE 696 provides an eight level vectored interrupt system. Interrupts provide the the means for a bus slave or peripheral device to obtain the services of a bus master in such a fashion that the master can return to the task which was in progress when service was requested. An interrupt controller slave may be included on the permanent bus master or on a separate bus slave. INT*, the general interrupt line, is used for communication between the interrupt controller and any master. Interrupt controllers vary all the way from single chips to entire front end processors.

Regardless of type, only one interrupt controller may exist on the bus. If additional controllers are required they must be either daisy chained or operate in a polled mode. A sINTA cycle acknowledges receipt of an interrupt request, INT*, however, a vectored interrupt may occur and be serviced by an interrupt controller without the assertion of INT*. Interrupt controllers need not assert INT*.

8. UTILITIES 25 lines

The system utilities are ordered essentially as they appear in IEEE 696, however, some headings are relocated in the interest of clarity.

A. System clock, phi, provides control timing for all bus cycles. It is always generated by the host processor. In cases where there are more than one MPU on the host processor the clock may be transferred when MPU's are transferred. This transfer must be synchronous and glitch free.

B. Clock is an asynchronous 2 MHz +/- 0.5 percent signal. It is intended for use by timers, baud rate generators, etc.

C. Reset Functions 3 Lines

1. RESET* resets all bus masters.

2. SLAVE CLR*, SLAVE CLeaR, resets all bus slaves.

3. POC*, power on clear, is asserted only during power up and forces assertion of both RESET* and SLAVE CLR*. Reset and slave clr are open collector lines.

D. MWRT, Memory WRiTe strobe, is the signal which provides the timing for memory write operations. MWRT must be generated at only on point in a system. The host processor is the preferred location for this generator. MWRT = pWR . -sOUT. Care must be exercised in generating MWRT so that the strobe has minimum delay from PWR*.

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E. PHANTOM* is an open collector line used to overlay slaves at the same address location. Phantom must inhibit both read and write operations in disabled slaves.

F. ERROR* is an open collector general error line which may be asserted when an error of any type occurs in the current bus cycle.

G. PWRFAIL*, PoWeR FAILure, indicates impending power failure. POC* clears PWRFAIL*. PWRFAIL* should be generated in the system power supply to insure that there is sufficient stored energy available for the system to go into cocoon mode. Cocoon mode means that operation is terminated in such a fashion that operation can be resumed upon restoration of power. This implies that no damage occur to stored data and system hardware. A proper power fail sequence insures that machine state is stored, disk heads unloaded, etc.

H. POWER 6 Lines plus 3 Lines?
Plus 3 lines? These three lines were formerly protect (bus pin 70) unprotect (bus pin 20) and sense switch disable (bus pin 53). These lines are now defined as ground in IEEE 696. The stated purpose for this redefinition was to provide low impedance grounds on both sides of both the board and edge connector. In actual practice, the impedance of these lines is likely to be higher than desirable because of their locations within the physical bus structure. Additionally, the assignment of pin 53 has been changed twice since the proposed specification was published in July of 1979. In the author's experience, inclusion of a ground on pin 53 produced numerous reports of various front panels and CPU's failing to operate with pin 53 grounded. This writer recommends that designers avoid using line 53 in new products. If this recommendation is followed, this lines will be available for reassignment for future bus expansion.

1. Ground 2 Lines (Ground is both signal and DC common for the bus).

2. +8 Volts 2 Lines (7 < +8 < 25 Vav < 11 V +8 is the primary supply for +5 regulators on the bus).

3. +16 Volts 1 Line (14.5 < +16 < 35 Vav < 21.5 V +16 is the primary supply for +12 regulators on the bus).

4. -16 Volt 1 Line (-14.5 > -16 > -35 Vav > -21.5 V -16 is the primary supply for -12 regulators on the bus).

Inspection of the instantaneous and average voltage limits established by IEEE 696 shows that three terminal regulators may be used with an unregulated capacitor input power supply. Very small minimum cost system configurations may lend themselves to this approach. Thermal and power efficiency considerations become quite important with larger systems. Let us consider the case of a system requiring 25 Amps of +8 supply. If the power supply delivers the 11 volt maximum average, our system is consuming 275 Watts to deliver 125 Watts of Vcc power to system logic. The remaining 150 Watts are dissipated as heat from our voltage regulators. If the power supply delivers 7.3 volts to the bus, our system is consuming 182.5 Watts to deliver 125 Watts of Vcc power to system logic. The remaining 57.5 Watts are dissipated as heat from our voltage regulators. The above examples do not include any losses occurring within our power supply. Reducing power dissipation within the system lowers the operating temperature of the system components with a corollary increase in their life expectancy. Additionally, power consumption is reduced not only for the system itself but also in the amount of power expended to provide air conditioning for the space in which the system operates. These are extremely important considerations in these times of decreasing energy availability and increasing energy costs. As with all good things, there is a cost. The power supply used in the second example provides a pre-regulated + 8 volts. The cost of using monolythic switching regulators to provide 7.3 volts +/- 0.250 volts is minimal when compared with the resultant savings in cooling requirements and power consumption of the system. Further efficiency may be

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attained by establishing a sub-set of IEEE 696 which would permit distribution of regulated +5 volts directly to system boards.

I. NDEF, 3 Lines, Not to be DEFined, are optional signal lines for use by individual manufacturers. These lines MUST be fully defined by any manufacturer using them. They MUST be provided with switches or jumpers to eliminate bus conflicts and their signals MUST be 5 volt TTL logic levels.

J. RFU, 4 Lines, Reserved for Future Use, may not be used for any purpose. These lines are reserved for bus expansion and may be defined in future revisions of IEEE 696.

This completes a brief overview of the functions and operation of the 100 lines specified in IEEE 696/S-100.

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5.000
.250
"X"
.107 D (2 pl.)
.250
5.125
.125

APPENDIX B

IEEE 696/S-100 Pin Assignments

01	+8 Volt	51	+8 Volt
02	+16 Volt	52	-16 Volt
03	XRDY	53	Ground
04	VI 0*	54	SLAVE CLR*
05	VI 1*	55	DMA 0*
06	VI 2*	56	DMA 1*
07	VI 3*	57	DMA 2*
08	VI 4*	58	sXTRQ*
09	VI 5*	59	A 19
10	VI 6*	60	SIXTN*
11	VI 7*	61	A 20
12	NMI*	62	A 21
13	PWRFAIL*	63	A 22
14	DMA 3*	64	A 23
15	A 18	65	NDEF
16	A 16	66	NDEF
17	A 17	67	PHANTOM*
18	SDSB*	68	MWRT
19	CDSB*	69	RFU
20	GROUND	70	GROUND
21	NDEF	71	RFU
22	ADSB*	72	RDY
23	DODSB*	73	INT*
24	PHI	74	HOLD*
25	pSTVAL*	75	RESET*
26	pHLDA	76	pSYNC
27	RFU	77	pWR*
28	RFU	78	pDBIN
29	A 5	79	A 0
30	A 4	80	A 1
31	A 3	81	A 2
32	A 15	82	A 6
33	A 12	83	A 7
34	A 9	84	A 8
35	DO 1	85	A 13
36	DO 0	86	A 14
37	A 10	87	A 11
38	DO 4	88	DO 2
39	DO 5	89	DO 3
40	DO 6	90	DO 7
41	DI 2	91	DI 4
42	DI 3	92	DI 5
43	DI 7	93	DI 6
44	sM1	94	DI 1
45	sOUT	95	DI 0
46	sINP	96	sINTA
47	sMEMR	97	sWO*
48	sHLTA	98	ERROR*
49	CLOCK	99	POC*
50	GROUND	100	GROUND

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