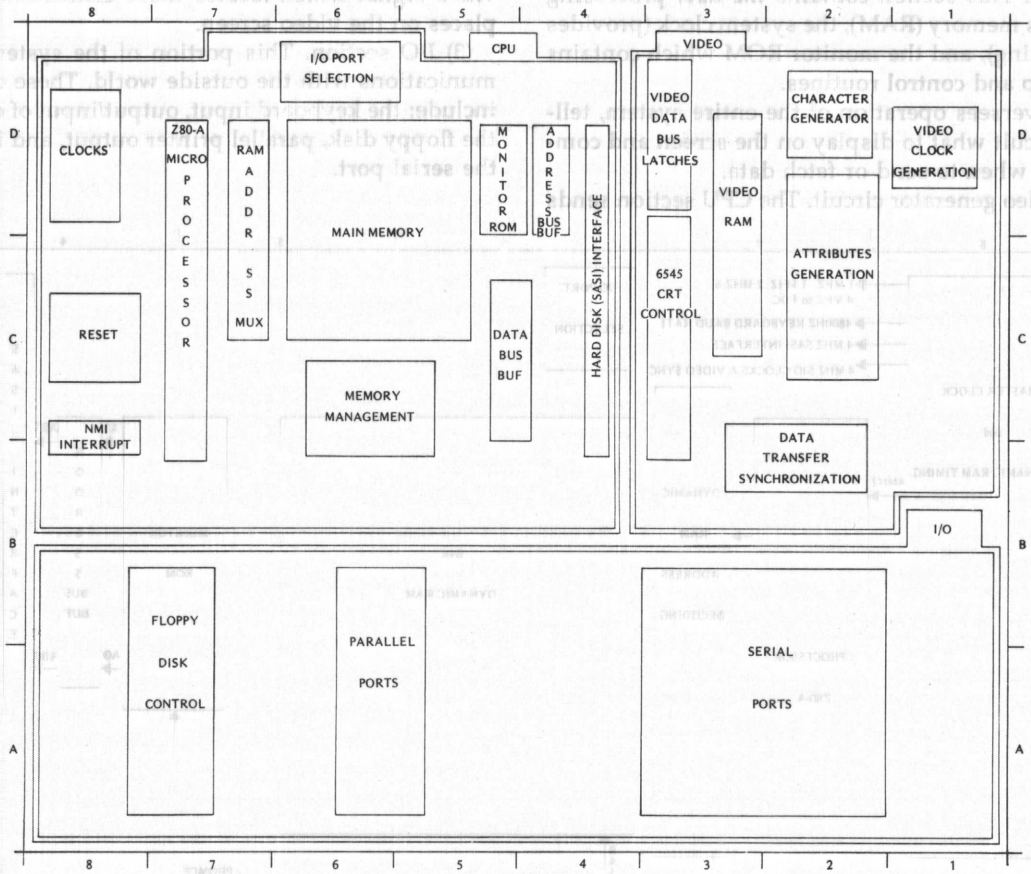
KAYPRO 10
THEORY OF OPERATION

By Eric Roby
Micro Cornucopia
P.O. Box 223
Bend, OR 97709



KAYPRO 10 BLOCK DIAGRAM

INTRODUCTION

Welcome to the Theory of Operation for the Kaypro 10. This manual covers the older Kaypro 10 (which does not contain a built-in modem or timer).

This theory of operation is designed to help you use Micro Cornucopia's Kaypro 10 schematic and to help you better understand the system. We assume you have a basic understanding of digital circuits, but we also do our best to define all of the abbreviated symbols (alphabet soup) for those of you whose command of computerese is a bit weak.

This theory of operation begins with a simplified diagram of the entire system. The blocks in this diagram are sized according to their relative importance. The diagram has the same basic layout as the schematic.

In our previous schematic package (for the Kaypro II and Kaypro 4) we divided the Kaypro into three sections -- CPU (central processing unit), video, and I/O (input/output). We do that again here. Each section begins with its own block diagram.

The diagrams are broken up into blocks, where each block represents a major function. Also, each block encloses the approximate area that the circuit occupies on the schematic. The blocks are arranged so that their grid coordinates correspond to the schematic coordinates of the related circuitry. The text which follows each block diagram, describes the parts and signals responsible for the circuit's function.

At the end of each section (CPU, video, and I/O), is a list of all the integrated circuits used in that section.

Note: There are a few arrows on the schematic that point toward letters and numbers in parentheses. The arrows are signal lines and the letters and numbers are the schematic coordinates of the signal destinations. We did our best to avoid this kind of thing, but we also wanted to keep the schematic as clear and readable as possible.

Active High/Active Low

A star (really an asterisk) following a signal label indicates that the signal is active low. For example, in the text, MREQ* is active low, but DRQ is active high. On the schematic we use the usual form for active low (a line above the signal name).

Note that a line is considered active when the ICs controlled by the line are turned on (i.e. selected). Some devices are selected when the voltage on their select pins is logic high (about 4 volts) while others (the ones with bubbles on their select inputs) are selected when the voltage on their select pins is logic low (about .7 volts).

Notice on the schematic that some of the signal names have lines over them. For instance, in quadrant B3, pin 25 of the video controller chip (U36) is enabled by the VIDCS (VIDeo Controller Select) line. The portion of the VIDCS line connected directly to pin 25 has a line over it, so it is called VIDCS NOT or VIDCS BAR. The video controller is selected (turned on) when the line goes low. In the text, we will call the line VIDCS*.

We also refer to logic '1' and logic '0'. Logic '1' is about 4 volts and logic '0' is about .7 volts.

CIRCUIT OVERVIEW

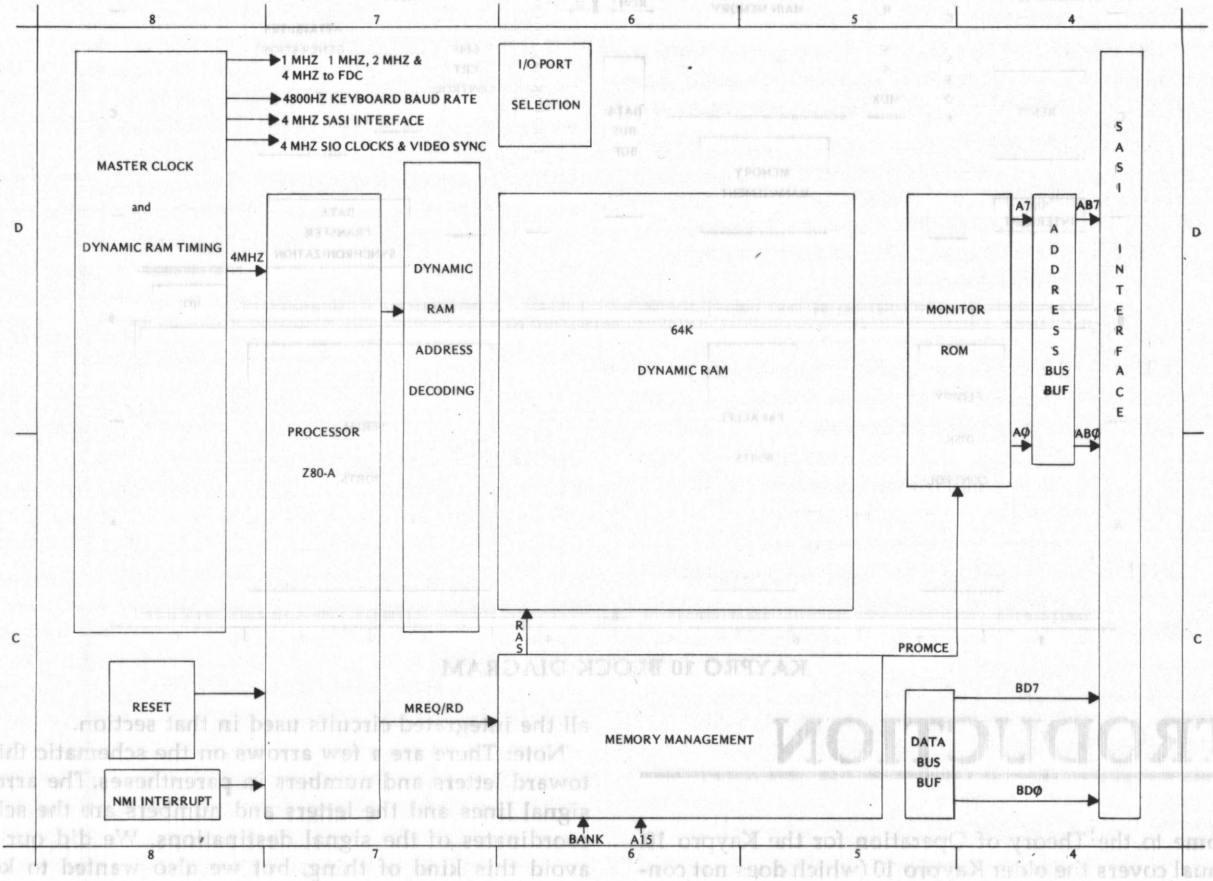
The KayPro design includes:

(1) CPU section with 64K of dynamic RAM and a system monitor in ROM. This section contains the data processing (CPU), fast access memory (RAM), the system clock (provides basic system timing), and the monitor ROM which contains the basic start-up and control routines.

This section oversees operation of the entire system, telling the video circuit what to display on the screen and commanding the I/O when to send or fetch data.

(2) Discrete video generator circuit. The CPU section sends characters along with information on where they should be displayed to this section. The video section then creates the video signal which locates those characters in their proper places on the video screen.

(3) I/O section. This portion of the system handles communications with the outside world. These communications include: the keyboard input, output/input of data to and from the floppy disk, parallel printer output, and input/output via the serial port.



CPU SECTION BLOCK DIAGRAM

CPU SECTION

The central processing unit of the KayPro 10 is a 4.0 MHz Z80-A using 64K of RAM for main memory. User programs and CP/M reside in this 64K of RAM (called bank 0). The monitor (contained in the EPROM U42) and video RAM lie in a separate bank of memory called bank 1. Only the lower 16K of main memory (bank 0) is switched out when bank 1 is accessed.

All serial input/output operations are interrupt driven.

RESET PULSE GENERATION-B8-

The power-on reset is a simple RC circuit. The way the circuit is designed, there is no way to guarantee that the contents of the system memory will be unchanged when the system is reset.

C31 must charge through the 10K resistor R12. Thus, the reset (RST*) signal will not go high until the power supply has had time to stabilize.

RST* is ORed with M1 to provide the I/O chips with an M1 reset (M1R*).

RAM TIMING AND ADDRESS DECODING-C6-C7-

The main memory is made up of eight 64K by 1 bit dynamic RAMs (random access memories).

These 4164 (or equivalent) RAM chips receive their 16-bit addresses in two chunks, eight bits at a time.

This is accomplished by multiplexing the 16 bit address bus into 8 bits. The signal responsible for timing this multiplex is the MUX signal. There are two other signals that are necessary for timing the addressing. CAS (column address strobe) and RAS (row address strobe) tell the RAM when the addresses are valid.

Timing-C8-

CAS and MUX signals are generated by shift register U49. The register is clocked by the 16 MHz clock. MREQ* or RFSH* will clear the shift register. MREQ* does this to synchronize the generation of CAS and MUX to the pending memory access. RFSH* does this to prevent generation of CAS and MUX during a memory refresh.

The MUX signal goes to the SELECT inputs of the two-to-

one multiplexers U48 and U47. A low on MUX selects the "A" inputs and a high selects the "B" inputs.

MASTER CLOCK -D8-

In a very real sense, the clocks are the heartbeat of the system. There are three clocks in this system, the 8116 baud rate clock, the video clock, (both of which will be described in later sections) and the master clock which controls the CPU and I/O sections.

16 MHz, generated by the master oscillator (U64), drives the pin 1 clock input of counter U59. Each output of this binary counter divides the 16 MHz by a successive power of 2. So, U59 pin 3 supplies 8 MHz, U59 pin 4 supplies the 4 MHz system clock, U59 pin 5 supplies 2 MHz and U59 pin 6 supplies 1 MHz.

A combination of 4 MHz, 2 MHz and 1 MHz clock frequencies are used to drive the floppy controller (U74).

KEYBOARD BAUD RATE -D8-

The 4800Hz clock for the keyboard baud rate is derived from U59 pin 6's 1 MHz output. First, U53 divides the 1 MHz input by 13 generating 76.9KHz on pin 15. This output becomes the input to pin 13 of U59. Again, U59 divides its input by powers of 2 providing 38.45KHz on pin 11, 19.225KHz on pin 10, 9.6125KHz on pin 9 and 4806Hz on pin 8.

INTERRUPT DECODE -B8-

The floppy disk controller (U74) controls the non-maskable interrupt (NMI*) line. DRQ and INTRQ outputs from the 1793 are ORed by U43 and ANDed with the HALT output from the processor. This output is connected to the Z80-A's NMI* (non-maskable interrupt) input (U28 pin 17). NMI* has the absolute highest priority within the Z80-A's interrupt scheme. Any other interrupt being serviced at the time that the NMI* line goes low will have to wait until NMI* has been serviced.

The I/O chips interrupt the processor via INT* (U28 pin 16), the maskable interrupt line. Maskable interrupts can be enabled and disabled via the software instructions EI (enable interrupt) and DI (disable interrupt). Non-maskable interrupts cannot be disabled.

MEMORY CHIP SELECT -C6-

RAS Generation -C6-

RAS (Row Address Select) is developed through a series of gates and control lines which resemble a route from NY to Washington D.C. via San Francisco. To begin the decode, inverted A15 and BANK are ANDed through U50 (pins 10 & 9). This output (pin 8) is inverted (U56) then ORed with RFSH through U50 (pins 5 & 4). The resulting output (pin 6) is ANDed with MREQ* (inverted through U56) through U50 (pins 1 & 2) to provide the select/deselect signal for RAS.

Bank Select -C6-

The monitor ROM and RAM are selected through the decode of BANK and A15. The initial circuit logic is the same as that used for RAS generation. BANK and inverted A15 are ANDed through U50 (pins 10 & 9). This output (pin 8) is ANDed with the output from U43 (pin 1). U43's output is the result of MREQ* and RD* being ORed from the Z80-A. A logic '0' at the output of U50 (pin 11) enables U41. This condition forces U41 to gate data from RAM onto the data bus. A logic '1' at pin 11 (U50) disables U41's outputs isolating the RAM outputs from the data bus.

To initiate a read from RAM, BANK must be a logic '0' or A15 must be a logic '1.' Also, both MREQ* and RD* must be active (low). To read the Monitor ROM, A15 must be a logic '0' and BANK must be a logic '1'. Conditions for MREQ* and RD* are the same as required for RAM. The monitor ROM occupies addresses 0000H-0FFFH.

MONITOR ROM -D4-D5

The monitor ROM is a 2732 (4K x 8 bit) EPROM. It handles low level disk operations, I/O and video operations, and power-up initialization for the Z80-A, floppy disk controller, CRT controller and the two SIO's.

SHUGART ASSOCIATES STANDARD INTERFACE (SASI) (J9) -C4-D4-

This interface is the only source of buffered address and data lines. The low 8 bits of the address line comes from buffer U38. The 8 data lines come from buffer U39. Only a few of the control lines at J9 are unbuffered. The SASI interface (J9) handles data transfer between the motherboard and the Winchester controller board.

CHIP UTILIZATION IN THE CPU SECTION

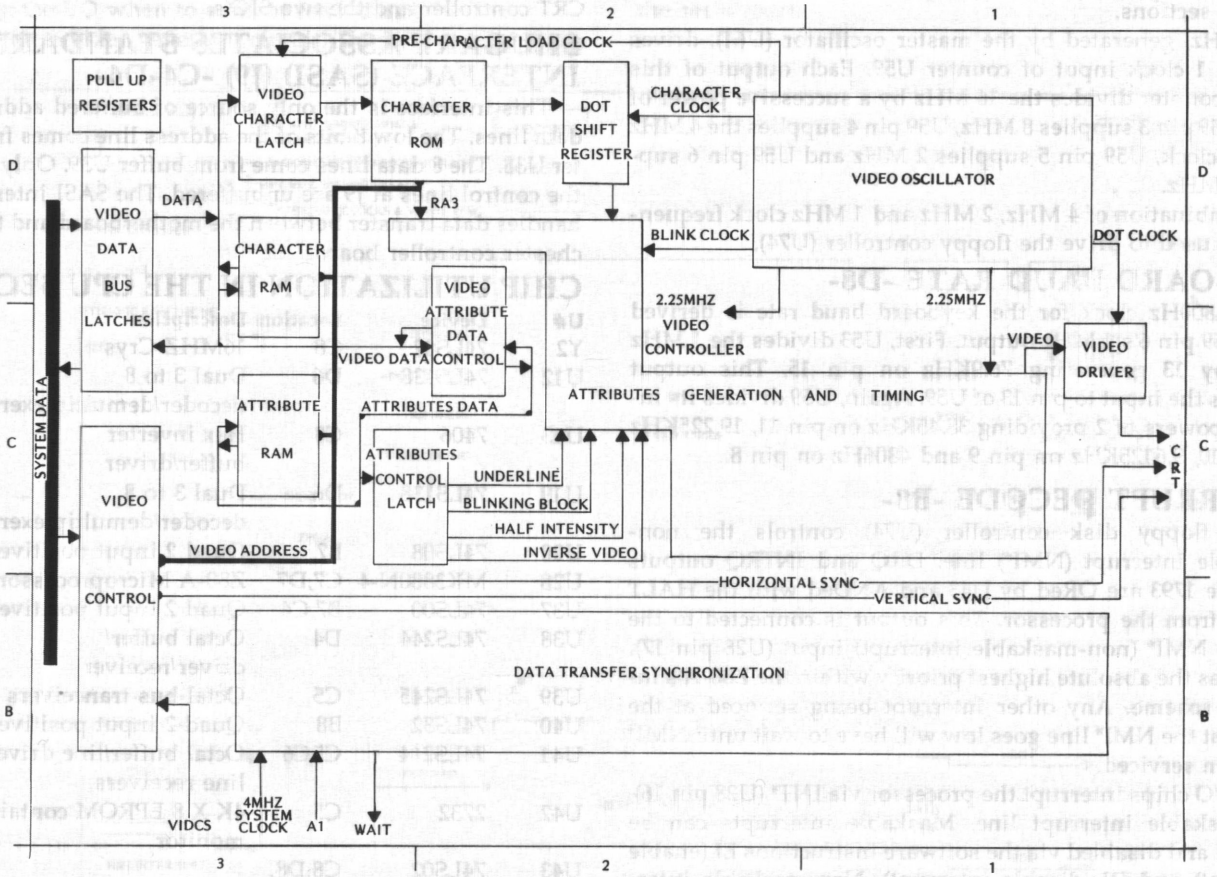
U#	Device	Location	Description
Y2	74LS02	C8	16MHZ Crystal
U12	74LS138	D6	Dual 3 to 8 decoder/demultiplexer
U13	7406	C8	Hex inverter buffer/driver
U19	74LS138	D6	Dual 3 to 8 decoder/demultiplexer
U20	74LS08	B7	Quad 2 input positive-AND
U28	MK3880N-4	C7,D7	Z80-A Microprocessor
U37	74LS00	B7,C4	Quad 2 input positive-NAND
U38	74LS244	D4	Octal buffer/ driver/receiver
U39	74LS245	C5	Octal bus tranceivers
U40	74LS32	B8	Quad 2 input positive-OR
U41	74LS244	C5,C6	Octal buffer/line drivers/ line receivers
U42	2732	C5	4K X 8 EPROM containing monitor
U43	74LS02	C8,D8, B8,B6	Quad 2 input positive-NOR
U47	74LS157	C7	Quad 2 to 1 line selector/multiplexer
U48	74LS157	D7	Quad 2 to 1 line selector/multiplexer
U49	74LS74	C8	Dual D flip-flop
U50	74LS00	C6,C5	Quad 2 input positive-NAND
U51,52	4164	C5,C6	64K X 1 Dynamic RAM
U57,58	4164	C5,C6	64K X 1 Dynamic RAM
U62,63	4164	C5,C6	64K X 1 Dynamic RAM
U68,69	4164	C5,C6	64K X 1 Dynamic RAM
U53	74LS163A	D8	Synchronous 4 bit binary counter
U56	74LS04	B5,B6	Hex inverter
U59	74LS393	D8	Dual 4 bit binary counter
U64	74HC04	C8,D7	Hex inverters

POWER CONNECTIONS

Power connections between the board and the power supply are shown on the schematic at J2. Once the power is on the board, the power is distributed as follows: U17, a 1488 RS-232 line driver, uses +/- 12 volts. +12 is supplied to the chip at pin 14 and -12 at pin 1. U17 changes TTL logic levels to

RS-232 voltage levels. Logic '0' is changed to -12 volts and logic '1' is changed to +12 volts. The floppy 1793 disk controller (U74) uses +12 volts in addition to +5 volts and ground. All the other chips require only +5 volts and ground. On the 14-pin ICs, pin 7 is grounded and pin 14 is tied +5V. On most of the 16-pin ICs, pin 8 is grounded and pin 16 is tied to +5V.

Pin	Use
1	ground
2	+12 power
3	no connection
4	+5 power
5	−12 power
6	Light Pen



VIDEO SECTION BLOCK DIAGRAM

VIDEO SECTION

The Kaypro 10 video section is based on the Synertek 6545 smart video controller. This chip generates the horizontal and vertical signals as well as addressing video RAM.

The following is a description of the 6545's control signals:

DE	indicates CRTC is providing addressing in the active display area.
VS	generates the vertical sync pulse for the CRT.
HS	generates the horizontal sync pulse for the CRT.
MA0-MA13	provides video RAM addressing.
RA0-RA3	provides row addressing to the Character ROM.
RS	selects either the address register (A0='0') or the data register (A0='1').
R/W	determines whether internal registers are to be written to or read from, a logic '0' defines a write command.
CUR	indicates a valid cursor address to external video logic.
EN	clocks data to and from the CRTC.
CCLK	2.25 MHz input derived from the external dot clock.
D0-D7	bidirectional data lines.

The 6545 (U36) has 18 programmable registers. The generation of the scan count, line count, frame count, horizontal sync, vertical sync, and horizontal blanking are set up by software. Registers 0 through 9 control all the timing functions. Registers 10 and 11 handle cursor control. Registers 0-11 can only be written to (the processor can't read them to verify their contents).

The following is the powerup initialization code for the 6545.

```
LD      A,0     ;(will select register 0)
OUT     1CH,A   ;(sends the 0 to the 6545's address
                ;register)
LD      A,6AH   ;(6AH is total displayed characters and
                ;nondisplayed character
                ;times [retrace] minus 1)
OUT     1DH,A   ;(sends the 6AH to the 6545 - register 0)
LD      A,1     ;(will select register 1)
OUT     1CH,A   ;(sends the 1 to the 6545 address register)
LD      A,50H   ;(50H defines the maximum number of
                ;horizontal displayed
                ;characters to be 80 [decimal])
```

```
OUT     1DH,A   ;(sends the 50H to the 6545 - register 1)
LD      A,2     ;(will select register 2)
OUT     1CH,A   ;(sends the 2 to the 6545 address register)
LD      A,56H   ;(56H defines the front porch [sync delay]
                ;and back porch
                ;[scan delay] to be 6 character times,
                ;thereby defining
                ;the horizontal sync position)
OUT     1DH,A   ;(sends the 56H to the 6545 - register 2)
LD      A,3     ;(will select register 3)
OUT     1CH,A   ;(sends the 3 to the 6545 address register)
LD      A,99H   ;(99H defines the horizontal sync pulse
                ;width to be 4 microseconds and the
                ;vertical sync pulse width to be 450
                ;microseconds)
OUT     1DH,A   ;(sends the 99H to the 6545 -register 3)
LD      A,4     ;(will select register 4)
OUT     1CH,A   ;(sends the 04H to the 6545 address
                ;register)
LD      A,19H   ;(19H defines the number of lines to be 24
                ;[decimal])
OUT     1DH,A   ;(sends the 19H to the 6545 - register 4)
LD      A,5     ;(will select register 5)
OUT     1CH,A   ;(sends the 5 to the 6545 address register)
LD      A,0AH   ;(0AH defines the fraction of character
                ;lines to be 10 [decimal],
                ;**note registers 4 and 5 define the vertical
                ;sync frequency to be 50Hz)
OUT     1DH,A   ;(sends the 0AH to the 6545 - register 5)
LD      A,6     ;(will select register 6)
OUT     1CH,A   ;(sends the 6 to the 6545 address register)
LD      A,19H   ;(19H defines the number of displayed
                ;character rows on the
                ;CRT to be 25 [decimal])
OUT     1DH,A   ;(sends the 19H to the 6545 -register 6)
LD      A,7     ;(will select register 7)
OUT     1CH,A   ;(sends the 7 to the 6545 address register)
LD      A,19H   ;(19H means NO vertical sync delay)
OUT     1DH,A   ;(sends the 19H to the 6545 -register 7)
LD      A,8     ;(will select register 8)
OUT     1CH,A   ;(sends the 8 to the 6545 address register)
LD      A,78H   ;(78H defines 6545 for 1 skew character
                ;and normal sync [non-interlace])
OUT     1DH,A   ;(sends the 78H to the 6545 - register 8)
LD      A,9     ;(will select register 9)
OUT     1CH,A   ;(sends the 9 to the 6545 address register)
LD      A,0FH   ;(0FH defines the maximum number of
                ;scan lines per character block to be 15
                ;[decimal] and controls operation of the
                ;row address counter)
OUT     1DH,A   ;(sends the 0FH to the 6545 - register 9)
LD      A,10    ;(will select register 10)
OUT     1CH,A   ;(sends the 10 to the 6545 address register)
LD      A,60H   ;(60H defines the cursor blink rate to be
                ;32 times the field refresh period,
                ;approximately 0.64 second)
OUT     1DH,A   ;(sends the 60H to the 6545 - register 10)
LD      A,11    ;(will select register 11)
OUT     1CH,A   ;(sends the 11 to the 6545 address register)
LD      A,0FH   ;(0FH defines the last scan line within a
                ;character block to be the 15th row)
OUT     1DH,A   ;(sends the 0FH to the 6545 -register 11)
```

**Note: Registers 12-15 are initialized to 00H at power up and are not used. Registers 16 and 17 can only be read (by the processor). They are used for light pen applications only.

VIDEO OSCILLATOR -D1-D2-

The video oscillator is the same type of circuit as the master oscillator in the CPU section. This oscillator runs at 18MHz and is used to generate all of the video frequencies. The dot clock (18MHz) and the video oscillator are one in the same.

PROCESSOR/VIDEO DATA TRANSFER -B2-B3-

Data transfer between the CPU and the 6545 is synchronized by the 4MHz system clock, VIDCS*, and address line A1. U33 receives the system clock at pin 3. U33 pins 5 and 8 are ANDed through U30, pins 5 and 4. As soon as U36 is selected (VIDCS*), the output of U30 pin 6 becomes a synchronized (system) pulse that enters the CPU into a WAIT state and clocks the enable pulse to U45 or U46 (depending on whether it is a read or write to video RAM).

CHARACTER CLOCK GENERATION -D1-

The dot clock (18MHz) provides the CLOCKA input to U66 a 4-bit binary counter. U66 then provides subharmonics of 18 MHz. U66 pin 12 supplies 9MHz, U66 pin 9 supplies 4.5MHz, U66 pin 8 supplies 2.25MHz and U66 pin 11 supplies 1.125MHz. Each of the outputs from U66 and the dot clock are ANDed through U61 (pins 1,2,4,5). The resulting output (pin 6), provides a low going pulse every 8 cycles of the dot clock. This pulse loads another byte (8 bits) into shift register U22. With this load pulse, the next active row (byte) of dots is loaded from the character ROM (U26) into the shift register.

VIDEO ADDRESS BUS -C3-D3-

The 6545 (U36) provides video addressing. MA0-MA10 (pins 4-14) addresses video RAM, RA0-RA3 (pins 35-38) does the row addressing to video ROM.

VIDEO RAM -C3-D3-

Two 6116 (2K x 8 bit) static RAM chips (U35 & U44) are used for video memory. The output enable (read) on these two (pin 20) is always active. Write enable (pin 21) for U44 is decoded from MA11 (U36 pin 15), VIDCS*, A1 and WR*. Write enable (pin 21) for U35 is decoded from RA4 (U36 pin 34), VIDCS*, A1, and WR*. Chip enable for U35 is decoded through the same control and address lines as write enable for U44. Chip enable for U44 is always active.

The 6116 decodes pins 18, 20 and 21 (CS,OE,WE) in the following manner: Since pin 20 is always active in this circuit, pins 18 and 21 determine RAM activity. When pin 18 is deselected (U35 only), the chip goes into the standby condition. When both 18 and 21 are selected, the output lines go to a high 'Z' state which sets up the chip for a write condition. When pin 18 is selected and pin 21 is deselected, the chips are set up for a read.

U35 and U44 correspond byte for byte. U44 stores the attributes (blinking, reverse, half intensity...) for the ASCII character stored at the corresponding address in U35. U35 is selected when MA11 is reset. U44 is selected when MA11 is set.

The transfer of attributes to and from U44 is accomplished through the octal bus tranceiver U54. The direction of data flow is determined by pin 1. A logic '0' on this pin gates data from the video data bus to the attribute data bus [i.e., a write to attribute RAM]. Likewise, a logic '1' on pin 1 gates data from the attribute data bus to the video data bus [i.e., a read from attribute RAM].

GENERATING ATTRIBUTES -C1-C2-D1-D2-

At power-up, all address locations within attributes RAM are initialized to zeros. If any of the low order four bits (D0-D3) is set to one, the corresponding output from octal latch U60 will go high.

You can try out the different character attributes directly from the keyboard:

[esc]B0	reverses video
[esc]C0	returns to normal video
[esc]B1	decreases the character block intensity
[esc]C1	returns normal intensity
[esc]B2	initiates the character blink
[esc]C2	returns the character to non-blink
[esc]B3	underlines the character block
[esc]C3	removes the underline

Any combination of attributes can be activated for any character. While an attribute is set, all characters entered into video RAM will have that attribute.

The attributes are generated as follows:

Underline is set by U60, pin 9. When the UNDERLINE line is high (bit 3 is set), the pixels in the 16th character row will be turned on (unless everything is reversed by reverse video).

Character blink is set by U60, pin 12. U9 multiplies the Vertical Sync period by 64. If blink is reset (normal) the output from U8 (pin 11) is always a logic '1'. This condition isolates the blink clock (U9) from the video data. But, as soon as BLINK is set the output from U8 is no longer a stable logic '1'. The blink clock now controls the video. Any characters sent to the screen while BLINK is set will turn off and on every 1.28 seconds.

Character intensity is set by U60, pin 6. If HALF intensity is set, U8 pin 8 goes low, drawing current from the video line, reducing video intensity.

Reverse/normal video is controlled by U60 pin 16. In normal video, the body of the character is formed by lit pixels while the rest of the dots are off. Reverse video simply means that the data going to the screen is reversed so that pixels which would be normally turned on are turned off and vice versa.

VIDEO/PROCESSOR INTERFACE -C3-D3-

Octal latches U45 and U46 are the link between the system data bus and the video data bus. U45 transfers data from the Z80 data bus to the video data bus while U46 transfers data from the video data bus to the Z80 data bus.

Chip select (pin 11) and output enable (pin 1) on both chips are decoded from A1, VIDCS*, WR* and RA4. As described in the Video Oscillator section, U45 is synchronized with the processor's write to video RAM and U46 is synchronized with a read from video RAM.

CHARACTER ROM -D2-D3-

A 2732 (4K x 8 bit) ROM chip, U26, holds the dot representation for the 128 ASCII characters. Each 7-bit ASCII character addresses a unique location within the character ROM. RA0 - RA3 define the active row within the character block and these four lines address 16 different rows. The ASCII character set only utilizes 14 of the 16 rows while the graphic set uses all 16.

In fact, the lower 2K of the ROM contains the ASCII character set. The upper 2K of ROM contains the graphic set.

The graphic set can be accessed by setting A11 (pin 21), otherwise the ASCII character set (lower 2K) is active. Zeros in the character ROM turn into lit pixels on the screen while ones in the ROM become unlit pixels.

CREATING A CHARACTER -D1-D2-

U31 latches the character byte from the video data bus. This 8-bit character becomes the most significant 8 bits of the address for the character ROM. Again, each character block is made up of 16 rows, with 8 bits per row. The 16 rows are addressed by RA0 -3 (Row Address 0 - 3).

The 8 dot bits (one scan row) are then latched from the character ROM into shift register U22. The bits are then shifted (one by one) out of U22 pin 9 by the 18 MHz dot clock. Then the bits go through U2 (pins 2,3), U14 (pins 4,6), U2 (pins 4,6) and U7 (pins 12,9). It is while the signal is going through these gates that the blink, underline, half intensity, and inverted video circuits get a chance to modify the bits before they reach the video output J1 pin 3.

Timing between U31, U26, and U22 is synchronized by the character clock and a modified version of the character clock. The modified character clock is generated from the outputs of U66 and the dot clock. Pin 8 and pin 9 are inverted and combined with pin 12 and the dot clock. These signals are ANDed through U61 (pins 9,10,12,13). The output (pin 8) enables U31, five dot clock cycles before the character clock loads U22 with the next active row (byte) of character dots.

GRAPHIC SET

The Kaypro 10 has two graphics modes. You can control individual pixels or you can draw a complete line. Both modes can be accessed through Console Command Processor (CCP) but because the CCP converts lowercase to uppercase, the right side of the screen is inaccessable by this method.

The screen is defined as a 100 x 160 pixel matrix. Pixels are numbered from 20H to 83H vertically and 20H to BFH horizontally. A coordinate of 20,20 corresponds to the upper left corner of the screen; 83,BF is located at the lower right corner. The reason for the unorthodox coordinates is that the monitor subtracts 20H. Pixels cannot be turned on where normal ASCII characters (0 - 127H) already exist.

To get a feel for the line drawing commands, try the following program. Each line drawing sequence defines two points by X,Y and X; Y; where X is the horizontal component and Y is vertical. All pixels between (and including) the two specified points are turned on.

Use DDT to enter the program listed below.

Use the "A" command to enter the following code at 100H:

```
MVI C,9     ;sets up for BDOS print string system call
LXI D,200   ;starting address where string is located
CALL 5      ;calls BDOS
RST 7       ;system control goes to DDT after program run
```

Now use the "S" command at 200H and enter the following string:

```
1A   ;single character control to clear the screen
1B   ;ASCII for [ESC] -special set to follow
4C   ;ASCII for L - two sets of X, Y coordinates to follow
30   ;ASCII for 0 - X component
60   ;ASCII for @  - Y component
30   ;ASCII for 0 - X' component
70   ;ASCII for p -Y' component
     ;the above draws the top side of the box
1B   ;ASCII for [ESC] - special set to follow
4C   ;ASCII for L - two sets of X,Y coordinates to follow
```

```
30    ;ASCII for 0 - X component
70    ;ASCII for p - Y component
70    ;ASCII for p - X' component
70    ;ASCII for p - Y' component
      ;the above draws the right side of the box
1B    ;ASCII for [ESC] - special set to follow
4C    ;ASCII for L - two sets of X,Y coordinates to follow
70    ;ASCII for p - X component
70    ;ASCII for p - Y component
70    ;ASCII for p - X' component
40    ;ASCII for @ - Y' component
      ;the above draws the bottom of the box
1B    ;ASCII for [ESC] -special set to follow
4C    ;ASCII for L - two sets of X,Y coordinates to follow
70    ;ASCII for p - X component
40    ;ASCII for @ - Y component
30    ;ASCII for 0 - X' component
40    ;ASCII for 9 - Y' component
      ;this draws the left side of the box
24    ;ASCII for $ - marks end of the string
```

Now enter G100 and a square should appear before your eyes.

To initiate the individual pixel mode make the following changes to the program: substitute 2A for 4C then only enter one X,Y coordinate per escape sequence.

For those with turbo pascal, the following will do the same trick:

```
PROGRAM Graphic (output);

Begin
  writeln (chr($1A);
  writeln (chr($1B),'L','0','@','0','p');
  writeln (chr($1B),'L','0','p','p','p');
  writeln (chr($1B),'L','p','p','p','@');
  writeln (chr($1B),'L','p','@','0','@')
End.
```

VIDEO CHIP UTILIZATION

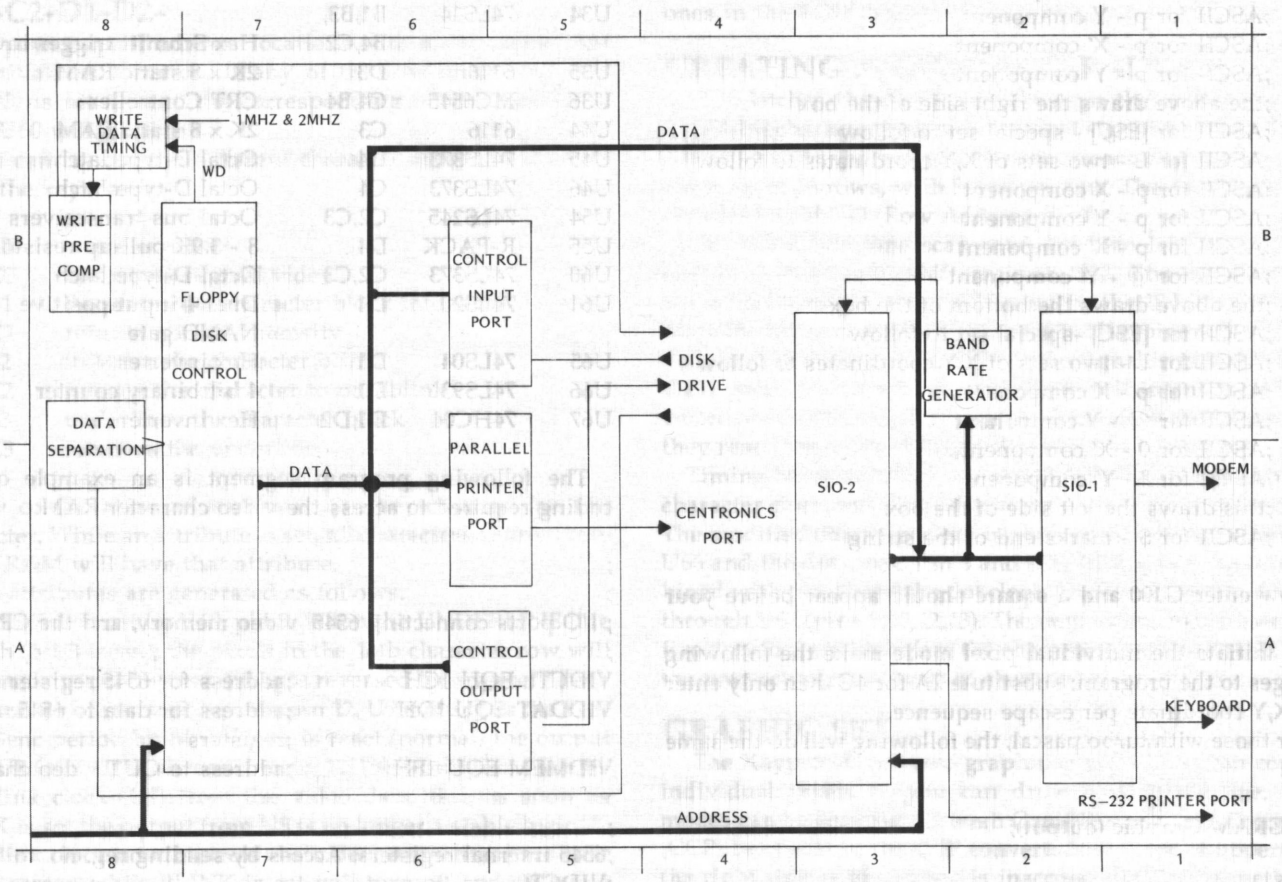
U#	Device	Location	Description
Y2	CRYSTAL	D2	18MHz crystal
U2	74S08	C2,D2,D3	Quad 2 input positive AND gate
U7	74LS74	C1	Dual D-type flip-flop
U8	74LS00	C3,D2,C2	Quad 2 input positive NAND gate
U9	74LS393	D2	Dual 4 bit binary counter
U14	74S86	C1,C2, D2,D3	Quad 2 input EXCLUSIVE OR gate
U15	74LS20	D2	Dual 4 input positive NAND gate
U17	74LS14	B2	Hex Schmitt trigger inverter
U21	74LS74	C1,C2	Dual D-type flip-flop
U22	74LS165	D2	Parallel load 8 bit shift register
U24	74LS74	B2	Dual D-type flip-flop
U25	74LS10	B2,B3	Triple 3 input positive NAND gate
U26	2732	D2,D3	4K x 8 Character ROM
U30	74LS08	B2,B3,C2	Quad 2 input positive AND gate
U31	74LS373	D3	Octal D-type latch
U33	74LS74	B3	Dual D-type flip-flop
U34	74LS14	B1,B3, B4,C2	Hex Schmitt trigger inverter
U35	6116	D3	2K x 8 static RAM
U36	MC6545	C4,B4	CRT Controller
U44	6116	C3	2K x 8 static RAM
U45	74LS373	D4	Octal D-type latch
U46	74LS373	C4	Octal D-type latch
U54	74LS245	C2,C3	Octal bus transceivers
U55	R-PACK	D4	8 - 3.9K pull-up resistors
U60	74LS373	C2,C3	Octal D-type latch
U61	74LS20	D1	Dual 4 input positive NAND gate
U65	74LS04	D1	Hex inverter
U66	74LS93	D1	4 bit binary counter
U67	74HC04	D1,D2	Hex inverter

The following program segment is an example of the coding required to access the video character RAM:

```
;
;
; I/O ports connecting 6545, video memory, and the CPU
;
VIDCTL EQU 1CH          ;address for 6545 register select
VIDDAT EQU 1DH          ;address for data to 6545
                        ;registers
VIDMEM EQU 1FH          ;address to OUT video chars to
;
;
;6545 internal registers. Access by sending reg. no. to
;VIDCTL
;
HIADD EQU 18            ;hi-byte, video memory
                        ;address
LOADD EQU 19            ;lo byte video memory address
STROBE EQU 1FH          ;6545 'strobe' command (send
                        ;after vid. add)
;
    LD A,18             ;set 6545 to hi address
                        ;reg. (#18)
    OUT (1Ch),A         ;by placing reg no. in
                        ;control port
    LD A,D              ;set hi byte, vid mem.
                        ;address
    OUT (1Dh),A         ;by putting value in
                        ;register port
    LD A,19             ;select lo address register
                        ;(#19)
    OUT (1Ch),A
    LD A,E              ;set it
    OUT (1Dh),A

    LD A,1Fh            ;strobe the address in
    OUT (1Ch),A         ;by outputting 'strobe'
                        ;command to
;                       ;control port
WAIT: IN A,(1Ch)        ;wait for 6545 to catch up
      OR A
      JP P,WAIT

    LD A,'E'            ;now output a character
                        ;to video
    OUT (1Fh),A         ;memory port
```



I/O SECTION BLOCK DIAGRAM

I/O SECTION

The Kaypro 10 uses two programmable serial I/O chips (SIO-1 and SIO-2) to handle the serial interfaces. One OCTAL Buffer/Line Driver/Receiver and two D-type latches handle the parallel traffic.

Side A of SIO-2 (U27) is the serial printer port. Side B is unused and its protocol and data lines are available at labeled solderpads on the board. Side A of SIO-1 (U23) is the MODEM port and side B is the keyboard port.

CHIP UTILIZATION FOR THE I/O SECTION

U#	Device	Location	Description
Y1	CRYSTAL	A3	5.0688MHZ Crystal
U3	74S04	A1,A2	Hex inverters
U4	MC1489	A1,B1	High voltage inverting line drivers
U5	74LS244	B6	Octal buffer/driver/receiver
U6	74LS74	A7	Dual D type flip-flop
U10	MC1489	A4,B1	High voltage inverting line drivers
U11	74LS373	A6	Octal D type latch
U13	7406	A5,B7	Hex inverter buffer/driver
U16	8116	A2,A3	Programmable baud rate generator
U17	MC1488	A1,A4, B1	High voltage inverting line drivers
U18	74LS373	A6	Octal D type latch
U20	74LS08	B7	Quad 2 input positive-AND
U23	MK3884	A1,B1	Z80 Programmable Serial I/O
U27	MK3884	A3,B3	Z80 Programmable Serial I/O
U29	74LS195	B8	4 bit parallel-access shift register
U32	74LS02	A6,A7	B8 Quad 2 input positive-NOR
U40	74LS32	A7,A8	Quad 2 input positive-OR
U72	74LS10	B8	Triple 3 input positive-NAND
U73	9216	B8	External data separator
U74	1793	A7,B7	Floppy Disk Controller

SERIAL I/O PORTS

	Port	Control	Date	Use
SIO-1	A	06	04	Modem (J3)
	B	07	05	Keyboard (J5)
SIO-2	A	0E	0C	Printer (J4)
	B	0F	0D	not used

PARALLEL I/O PORTS

U#	Port	Use
U18	18	Centronics port (J6)
U11	14	System bit port (J8)
		bit 0, drive A select
		bit 1, drive b select
		bit 2, side 1 select
		bit 3, centronics data strobe (J6)
		bit 4, disk drive motors
		bit 5, double density enable
U5	14	bit 6, centronics ready flag (J6)
		bit 7, bank select

I/O SELECT/DECODE -D6-

Each major chip in the I/O (input/output) section (SIO-1, SIO-2 and the Floppy Disk Controller) monitors address lines A0 and A1. The processor uses these two address lines to tell each I/O chip which control or data register it wants to read from or write to.

U19 and U12 are 3-to-8 decoders that select which chip is enabled. The decoders themselves are selected by address line A7 so all port addresses lie between 00H and 7FH. U12 and U19 are synchronized with M1R*, however, only U19 is selected by IORQ*. U12 generates only the 1793 select signal.

The use of U19's outputs is shown below.

Output #	Use
0	Set baud A strobe
1	SIO-1 chip enable
2	Set baud B strobe
3	SIO-2 chip enable
4	no connection
5	system port
6	Centronics port
7	Video chip enable

SERIAL I/O -A2-A3-

SIO-2 has higher priority than SIO-1 in the daisy chain. This means an interrupt from the serial printer has precedence over the modem or the keyboard. The baud rate for the RS-232 printer port and modem are provided by U16 a dual, programmable, divider designed to be used as a baud rate generator.

PARALLEL I/O -A6-B6-

Octal buffer (U5) is used as a system input port. Octal latch (U11) handles the output. Together, U5 and U11 monitor and send control signals to the printer, floppy disk drives and the bank select line required for ROM and RAM.

To enable U5 (control input port) RD* and SYSPRT* must be low. An I/O read from address 14H initiates the proper control levels on RD* and SYSPRT*.

To enable U11 (control output port) WR* and SYSPRT* must be low. An I/O write to address 14H initiates the proper control levels on WR* and SYSPRT*.

To enable U18 (centronics printer port) WR* and PDATA* must be low. An I/O write to address 18H latches a byte into U18 for transfer to the printer.

DISK DRIVE CONTROLLER PORTS

Addr.	In	Out
10H	status	command
11H	track	track
12H	sector	sector
13H	data	data

INTERRUPTS

The I/O ports in the KayPro are assigned priority by hardware design. The floppy disk controller has the highest priority so it controls processor's NMI input. The other I/O ports are daisy-chained together using the Z80 I/O IEO (interrupt enable out) and IEI (interrupt enable in) pins.

The highest priority chip has its IEI tied to 5 volts. The IEO from this chip goes to the IEI of the next highest priority chip. This continues for all the chips in the priority chain with the IEO of the last chip left unconnected. This way all the I/O chips use the INT* input to the processor with the interrupt priority resolution taken care of by the I/O devices themselves. The priority chain is as follows:

1. Floppy disk controller ports
2. SIO-2 ports
3. SIO-1 ports

BAUD RATE GENERATION-A2-A3-

U16 is a programmable baud rate generator. All that it requires to provide software selectable baud rates for the SIO is a 5.0688 MHz crystal and access to the data bus. Only the lower nibble (4 bits) of the data bus is used, and these 4 bits set the baud rate for either port A or port B.

The address bus is decoded by U19 to provide the baud rate set strobe. When U16 sees a strobe on one of its STBX inputs, it examines D0-D3 and generates the selected frequency at the FX output. The baud rates are listed below.

Baud	D0-D3	Baud	D0-D3
50	00H	1800	08H
75	01H	2000	09H
110	02H	2400	0AH
134	03H	3600	0BH
150	04H	4800	0CH
300	05H	7200	0DH
600	06H	9600	0EH
1200	07H	19200	0FH

As an introduction to the SIO, the following list provides the function of some of the SIO pins.

B/A*	Selects between channel A and channel B
C/D*	Selects port use as control (C) or data (D)
CE*	Enables the internal data bus tranceivers
M1* and IORQ*	Interpreted by the SIO as an interrupt acknowledge
RST*	Disables RCVR and XMTR functions and clears all control registers
TxCA and TxCB	Transmitter clocks
RxCA and RxCB	Receiver clocks

In the KayPro the transmitter and receiver clocks are tied together so that the baud rate must be the same in both directions.

SIO-1 Channel B is dedicated to the keyboard. The keyboard for the KayPro outputs serial data at 300 baud. Only two of the SIO's pins are used for the keyboard, transmit data and receive data.

The transmit data line is used only for the keyboard bell. The system monitor sets the baud for channel B to 300 baud on initialization. All handshaking lines are ignored.

SIO-2 Channel A is used for an RS-232 port. This port is referred to by software as 'TTY'. This port is initially setup to handle 8 bits/character, 1 stop bit, no parity. The configuration program that comes with the KayPro only sets the baud

rate. It doesn't let you set the number of bits/character, the number of stop bits, or parity.

SIO-2 Channel A uses nearly all of the RS-232 handshake lines. Following is a list of the DB-25 (J4) pin usage.

DB-25 pin	Mnemonic	Description
1		Frame ground
2	TxD	Transmit data
3	RxD	Receive data
4	RTS	Request to send
5	CTS	Clear to send
6	DSR	Data set ready
7		Signal ground
8	DCD	Data carrier detect
20	DTR	Data terminal ready

On the KayPro, frame and signal ground are tied together and to the ground bus. Pin 6 (DSR) is tied to 5 volts so it is high as long as the system is powered up. The other pins connect through line drivers to the SIO chip. U17 contains line drivers which output +12V and -12V RS-232 line levels for the RTS, DTR, and TxD lines. U4 and U10 contain RS-232 line receivers. It changes RS-232 signal levels to TTL signals for the SIO.

Software control of the SIO

The SIO is actually a more complex chip than the Z80. Programming it is not a trivial project, and I recommend that you find someone local who has done it a few times (preferably successfully) to help you get started. You'll save yourself a lot of time and frustration this way.

There are manuals on the SIO put out by the chip's manufacturers. Zilog's manual is complete, but it is no more readable than any of the others.

Basically, you need to send a string of bytes to the SIO control port (also called the status port) for side A. (Remember that side B of the SIO-1 is dedicated to the keyboard so don't mess with that unless you don't plan to use your keyboard.)

SIO-1 port A control is called port 06 in the KayPro. If you want to output new control information to that port, you would do something like:

```
LD    A,18H   ;(18H will reset the SIO)
OUT   06,A    ;(send the 18H to the SIO's register 0)
LD    A,01H   ;(01H will tell the SIO you want register 1)
OUT   06,A    ;(output the 01H to the SIO control port)
LD    A,00H   ;(00H in register 1 puts SIO in no-
                interrupt mode)
OUT   06,A    ;(send the 00H to register 1)
LD    A,04H   ;(04H will tell the SIO you want register 4)
OUT   06,A    ;(output the 04H to the SIO control port)
.
.
. (see figure 1 for complete example)
```

If you want to reconfigure the SIO, you first need to write to the control register which steers the following byte to the correct destination. This is control register WR0. When you output a byte of data to KayPro port 06, the data goes directly to the SIO-1's control register 0.

When you output a byte to control register 0, you can either use that byte as a direct command for the SIO, or you can use the byte to select another register (1-7).

You can use bits D0-D2 to indicate the target register for the next byte or you can use bits D3-D5 to specify a direct command to control register 0.

Register 0 command codes.

D3	D4	D5	COMMAND
0	0	0	select register with D0-D2
0	0	1	transmit abort (for SDLC mode)
0	1	0	reset status interrupts
0	1	1	reset one channel (the selected channel)
1	0	0	enable interrupt on next char. received
1	0	1	reset transmitter interrupt pending
1	1.	0	reset error latches (18H in line 1 above)
1	1	1	return from interrupt (channel A only)

For most purposes, only 000 is used. Bits D6-D7 reset the CRC checkers and generators and are usually left at 00 also. The following table illustrates the pointer to each control register and its use.

WR1	interrupt mode select
WR2	interrupt vector
WR3	receiver parameters
WR4	parity/clock multiplier/stop bits
WR5	transmit parameters
WR6	for synchronous use
WR7	for synchronous use

Common Configurations for KayPro Communications

Register	Bits		Function
WR3	D7	D6	Receiver Bits/Character
	0	0	5 bits/char
	1	0	6 bits/char
	0	1	7 bits/char
	1	1	8 bits/char
		D0	Receive Enable (when set to 1)
		D5	Auto enable on CTS (when set to 1)
WR4	D3	D2	Stop Bits
	0	0	none (synchronous)
	0	1	one stop bit (most common)
	1	0	one and a half stop bits (least common)
	1	1	two stop bits
	D1	D0	Parity
	0	0	no parity
	0	1	odd parity
	1	1	even parity
		D6	16X clock (should be always set to 1)
WR5		D7	Assert DTR (when set to 1)
	D6	D5	Transmit Bits/character
	0	0	5 bits/char
	1	0	6 bits/char
	0	1	7 bits/char
	1	1	8 bits/char
		D3	Transmit Enable (when set to 1)

So, let's look at a complete initialization of the SIO (a completed version of the above example).

Figure 1. SIO Initialization

```
LD      A,18H   ;(18H will reset the SIO)
OUT     06,A    ;(send the 18H to the SIO's register 0)
LD      A,01H   ;(01H will tell the SIO you want register 1)
OUT     06,A    ;(output the 01H to the SIO control port)
LD      A,00H   ;(00H in register 1 puts SIO in no-
                ; interrupt mode)
OUT     06,A    ;(send the 00H to register 1)
LD      A,04H   ;(04H will tell the SIO you want register 4)
OUT     06,A    ;(output the 04H to the SIO control port)
LD      A,45H   ;(45H in register 4 means 16X clock, 1 stop
                ; character,
OUT     06,A    ;(send the 00H to register 1)
LD      A,03H   ;(03H will tell the SIO you want register 3)
OUT     06,A    ;(output the 03H to the SIO control port)
LD      A,41H   ;(41H in register 3 means 7 bits/RCV
                ;bit, odd parity)
                ; non-synchronous, receiver enabled)
OUT     06,A    ;(send the 41H to register 3)
LD      A,05H   ;(05H will tell the SIO you want register 5)
OUT     06,A    ;(output the 05H to the SIO control port)
LD      A,A8H   ;(A8H in register 5 means DTR asserted,
                ; 7 bits/XMIT
                ;character, transmitter enabled)
OUT     06,A    ;(send the A8H to register 5)
                ;(set up baud rate generator)
LD      A,07H   ;(07H will set the baud rate generator to
                ;1200 baud)
OUT     00,A    ;(send the 07H to the baud rate generator)
```

For 7 bits/character, even parity, D1 of WR4 must be set to 1.

For 8 bits/character, no parity, set D0 of WR4 to 0. Set D7 and D6 of WR3 both to 1 and set D5 and D6 of WR5 also both to one.

FLOPPY DISK CONTROLLER-A7-B7-

The KayPro 10 uses a 1793 floppy disk controller, U74. The 1793 only needs two external chips. It requires a 1 Mhz clock to operate. It uses four signals from the floppy disk drives—Track 0, Write Protect, Index, and the Raw Data from the read head. The controller provides the floppy disk drives with some control signals and the rest are provided by the system bit port. The signals originating from the controller are Write Gate, Step, and Direction. The write data and precompensation information are fed to one of the external chips which provides the properly timed write data.

DATA SEPARATION-A8-

The data stream from the floppy disk is made up of two components, clock and data. The 1793 is not capable of separating these two components, so U73 is used to remove the clock pulses from the data stream. U73 provides the separate data and clock signals to the 1793.

WRITE PRECOMPENSATION-B8-

U29, a shift register, is used for write precompensation. It uses early and late signals from the 1793 to determine the direction of shift. If both early and late are low, the shift register is loaded through the B input. An early signal causes the data to be shifted early, which means it will arrive at the write head sooner.

Precompensation is required for double density formats. Precompensation usually is used to adjust for the difference in disk speed between the inner and outer tracks, however, the Kaypro 10 uses precompensation on all tracks.

Shift register (U29) is loaded by the write Data (WD) output (pin 31) of the 1793. The timing and duration of the signal generated by the WD line is controlled by combining a 2MHZ signal (pulse width) with an inverted 1MHZ signal (timing) and clocking the result through U29 with the 4 MHz on pin 10.